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(71) Applicant: TEKSTAR SYSTEMS CORPORATION [US/US]; 2415 Parkview Road, Middleton, WI 53562 (US).

(72) Inventor: ELAM, Daryl, B. ; 8503 Fairway Place, Middleton, WI 53562 (US).

(74) Agent: CURFISS, Robert, C.; Andrus, Sceales, Starke & Sawall, 100 East Wisconsin Avenue, Suite 1100, Milwaukee, WI 53202 (US).

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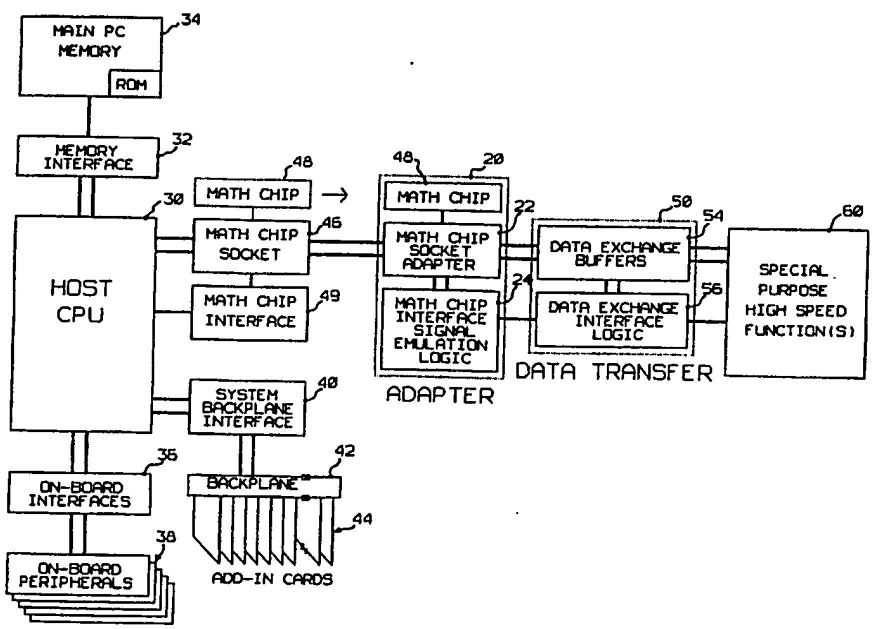

(57) Abstract

Logic interface circuitry for bypassing the standard backplane bus (40) of a host computer (30) permits the transmission of data between the host computer (30) and special purpose high-speed function add-in peripherals (60). The data is transmitted at the rate it is generated by the host computer (30) and the add-in peripheral (60).

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+ DESIGNATIONS OF "SU"

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INTERFACE SYSTEM FOR DATA TRANSFER WITH REMOTE PERIPHERAL INDEPENDENTLY OF HOST PROCESSOR BACKPLANE

BACKGROUND OF THE INVENTION

Field of the Invention

The invention relates to a means and method for bypassing standard computer interface backplanes in order to increase the data transfer rate between the host computer and a remote system.

Description of the Prior Art

It has long been recognized that the use of personal computers (PCs) is generally limited by their inability to perform certain functions in a high-speed, efficient manner. This leaves the users of certain special purpose high-speed function add-in peripherals with the choice of adapting to a slow, cumbersome processing operation, or of using a far more expensive mini-computer or mainframe system at many times the cost of a PC whenever efficiency and/or speed is a key factor in the operation.

The backplane bus bandwidth is the most significant factor in restricting the usefulness of high-speed add-in system components which require use of the backplane to communicate with a system central processing unit (CPU). Such components are most efficient when data transfer can be accomplished at the data transfer rate of the CPU rather than at the transfer rate of the backplane. The bandwidth limitations are most pronounced when there is a large discrepancy between the peak data transfer rate capabilities of the system CPU and the backplane bus. Over the years, this discrepancy has become greater and greater, as new generations of new CPUs are introduced far more often than new generations of backplane buses. As CPU capability and speed increase, the backplane becomes the limiting factor in using the CPU with add-in systems to perform more complex tasks.

The primary reason that backplane design lags CPU development is the requirement for standardization. The Institute of Electrical and Electronic Engineers (IEEE) has established standards for backplane architecture which permit numerous manufacturers to design add-in systems for a variety of host CPUs with a high degree of certainty that the mixing and matching of such systems and CPUs will result in an operable system. While this approach assures flexibility, the tradeoff is a lack of efficiency.

In an effort to overcome this, more of the functions benefiting from high speed data transfer are being incorporated onto the host CPU board to avoid using the backplane bus as a communication device. Examples that have become accepted are numerics co-processor chips, mass storage controllers, video controls and local network interfaces. Physical limitations of the host CPU board render continuing movement in this direction impractical, if not impossible.

The present invention is intended to permit a wide variety of add-in systems to operate at a high data transfer rate by bypassing the backplane of the host processor without the requirement that the add-in system be physically located on the CPU board. The invention takes advantage of the availability of the functional signals connected to and available at sockets generally provided in the standard CPU board. The invention uses the available sockets to permit development of a communications interface to shunt around the backplane bus. An adapter and data processing logic are connected to a selected data access point to provide a data transfer path for connecting the host CPU with the add-in systems. By

using the invention, the data transfer rate can be increased by a factor approaching a magnitude over the capability of the backplane.

SUMMARY OF THE INVENTION

The present invention comprises a means and method for circumventing the limitations of the data communications speed of standard computer interface buses. The backplane bus restricts the usefulness of a certain class of add-in system components, generally in the form of add-in circuit boards, which use the backplane bus to communicate with the system CPU. This class is characterized primarily by the desirability to tranfer data to and/or from the system CPU as quickly and efficiently as possible. The invention utilizes the standardization of the signal connections in the system CPU and/or other peripheral sockets in the CPU board as a convenient location to access the required signals and shunt around the system backplane bus. This may be accomplished by inserting a small socket adapter into the selected socket and then relocating the displaced chip into a similar socket provided on the adapter. In this manner, the protocol established between the displaced chip and the host CPU is maintained and the adapter borrows the data available from the CPU at the socket. Thus, the accessing schemes and handshake protocol of the original, now displaced chip are preserved and the host CPU operates as if it is communicating only with the chip. The signals which are available are then lifted from the socket by the adapter for communicating with the remote add-in system.

In an alternative embodiment, the interface includes dedicated interface logic which duplicates the protocol and accessing schemes of the host CPU or the

displaced chip. This permits direct communication between the host CPU and the adapter circuitry without the use of the displaced chip.

The adapter provides a hard wired system which electrically connects the required signals available at the selected data access point to a remote add-in system to provide a high speed data transfer bus. The only additional electrical connections required other than those available at the selected socket may be the DC power and ground lines which can be taken directly from the standard backplane.

By way of example, the standard PC backplane, known as an Industry Standard Architecture (ISA) backplane, or alternatively, as the IBM PC-AT bus, provides a data path which is 16 parallel bits, the maximum recommended backplane clock speed being 8 megahertz (MHz). The fastest backplane transfers require 4 clock cycles, yielding a peak bandwidth of 4 megabytes per second. Using the present invention with a 33 MHz clock speed requires the same 4 clock cycles per transfer as is standard. The invention yields a data transfer rate of 33 megabytes per second, an over 8-fold improvement. In the example, an Intel 80386 microprocessor is used. The invention may be adapted to interface with most available microprocessors, numeric chips and other generally available sockets or access points, provided the CPU provides at the socket all signals required by the add-in board. The adapters may be stacked or "piggy-backed" on top of one another to permit multiple add-in boards simultaneously utilizing the same socket. The particular function of the add-in system is incidental to the invention as long as the signals required to operate the add-in system are available at the adapter socket.

The various advantages and features of the

invention will be readily apparent from the accompanying drawings and description of the preferred embodiment.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a general block diagram of a host processor in combination with a special purpose high-speed function peripheral add-in and an interface unit incorporating the teachings of the present invention.

Fig. 2 is a detailed flow chart of the interface device illustrated in Fig. 1.

Fig. 3 is a diagram of a typical (prior art) state machine which may be an integral part of the interface device shown in Figs. 1 and 2.

Figs. 4-13 are a schematic diagram of a data transfer interface device made in accordance with the teachings of the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENT

As shown in Fig. 1, the present invention includes an adapter 20 and a data transfer device or circuit 50. In the embodiment illustrated, the CPU of a standard PC such as, by way of example, an IBM PC-AT compatible system having an Intel 80386 microprocessor 30, includes a standard memory interface 32 and main PC memory 34, typical onboard interfaces 36 and typical onboard peripherals 38. A standard system backplane interface 40 is used to provide communication between the CPU 30 and the backplane 42 for providing data transfer to and from the add-in cards 44.

Typically, the PC will include numerous peripheral sockets such as, by way of example, the extended math chip (EMC) socket 46 adapted for receiving a standard numerics chip 48 such as, by way of example, the Weitek 3167 or the Intel 80387 math

chip. The math chip interface logic circuitry 49 is also provided to control communication between the PC and the math chip.

The subject invention is specifically adapted for connecting the CPU 30 to special purpose high-speed function (SPHSF) add-in systems 60, bypassing the system backplane 42 by utilizing the direct connections to the full speed CPU signals via the math chip socket 46. The math chip socket of the CPU is a convenient place to gain access to the signals needed for the high-speed direct interface. However, the adapter could also be placed directly on the CPU chip or at any other convenient location on the main CPU circuit board where direct access to the required CPU signals can be gained.

As shown in Fig. 1, adapter 20 includes a math chip socket adapter 22 which is connected directly to the math chip socket via a standard plug and socket arrangement which is designed to mate with the math chip socket 46 provided in the PC. The adapter provides a direct communication link between the math chip socket and the data transfer device 50. The adapter can physically be plug compatible with the math chip socket and coupled to ribbon cables or the like which are, in turn, in direct communication with the data transfer device 50. As an option, the math chip 48 may be plug compatible with the adapter. The math chip interface logic 24 may be located on the adapter 20 or may be remote and coupled via the cable.

The protocol and accessing schemes provided in the math chip is preserved in one of three alternative methods when in utilizing the present invention. In the first, the math chip 48 is simply removed from the math chip socket and reinserted in the math chip socket adapter 22 in parallel with the data

transfer logic device 50, whereby the PC continues to communicate directly with the math chip and the adapter "picks off" the signals in a passive or non-invasive manner and transmits them to the data transfer circuit 50. In the second method, the math chip interface signal emulation logic circuit 24 emulates the accessing and signal protocol scheme of the math chip to duplicate those of the math chip, whereby the CPU communicates with the adapter as if it were a math chip. In a third method and as described herein, the math chip is only emulated to the degree necessary to permit communication with the CPU. The system has distinct interface characteristics, only emulating as much as necessary of the math chip to permit communication.

The physical configuration of the socket adapter is not critical to the function of the invention except for the requirement that the pin and socket arrangement of the adapter must be compatible with the selected data access point on the CPU board. The adapter may be a structural part of the special purpose circuit board including the math chip interface signal emulation logic 24 and the data transfer logic 50, or it may be remote from the board and connected to it by using cables. Likewise, the SPHSF 60 may be plugged directly into the adapter and/or data transfer board or may be plugged into a socket which then communicates via cable with the data transfer board. The signals to be transmitted from the host CPU 30 to the SPHSF 60 are communicated to the data transfer device 50 via the adapter 20. The signals to be transmitted from the SPHSF 60 to the CPU 30 are communicated to the data transfer device 50 directly from the SPHSF 60. Data exchange buffers 54 receive the data at the rate it is generated and supply it to

the receiving processor on demand at the rate it can be used. This permits use of asynchronous CPUs and SPHSF The data exchange interface logic device 56 provides interfacing and control logic for controlling the buffer function in response to the CPU 20 and SPHSF 60.

An expanded diagram of the data exchange circuitry 50 is illustrated in Fig. 2. As there shown, three primary communication paths exist between the adapter 20 and the data exchange circuitry 50. The first is a host PC data bus 25 which directly links the CPU signals present at the math socket with the exchange circuitry 50. The host PC control bus 26 provides a path for communication of the various control signals between the CPU 30 and data exchange interface logic 56. In addition, PC address bus 27 and "selected" signal line 28 provide for the address and selection signals to be transmitted between the PC and the data exchange circuitry via adapter 20. The data transfer and control signals between the data exchange circuit 50 and the SPHSF 60 are provided at buses 51 and 52 and 33, respectively. The data transfer rate is at the respective processing rate of the SPHSF 60 and the host CPU 30. By using this scheme, the CPU and the SPHSF can transfer data to and from each other at the speed of each of the systems, rather than at the speed permitted by standard backplane architectures.

By way of example, by using the adapter 20 and the data transfer circuitry 50 of the present invention, an over 800% advantage can be gained in data transfer rate (DTR) over that available from a standard IBM PC-AT bus. Using the following formula to determine data transfer rate in megabytes per second (MBs):

$$DTR = \frac{R \times W \times (1-L)}{C \times 8}, \text{ where}$$

R = the bus clock rate in megahertz,
W = the width of the data bus in bits,
L = the loss due to refresh,
C = clock periods per transfer, and
8 = the number of bits per byte.

Assuming the fastest uni-directional software instructions are used for data transfer and that these are the "string move" instructions of the Intel 386 CPU for an IBM PC-AT such as, by way of example, "REP MOVSW", and the effects of the PC main memory refresh are equal in both cases, the following calculations can be made:

For the PC-AT Bus:

$$DTR = \frac{R \times W \times (1-L)}{C \times 8}$$

$$= \frac{8 \times 16 \times (1-.03)}{4 \times 8}$$

$$= 3.88 \text{ mbs}$$

Data Exchange of the Invention:

$$DTR = \frac{RxWx(1-L)}{Cx8}$$

$$\frac{33x32x(1-.03)}{4x8}$$

$$= 32.01 \text{ mbs}$$

Thus, for the specific example, the invention provides an increase in data transfer rate of

$$\frac{32.01}{3.88}, \text{ or } 825\%$$

Basically, the data exchange circuit 50 operates as a buffer for storing data produced by the host CPU 30 and the SPHSF 60. The buffers 54 collect information as quickly as it is produced and release it on demand, as needed. The interface logic 56 monitors the SPHSF 60 and the buffers 54 to determine when the buffers are ready to receive data and when the buffers have data available to transfer relative to the SPHSF. The host CPU interface logic 57 communicates with the math chip socket adapter and through it with the host CPU 30 to similary monitor and determine when the buffers are ready to receive and/or transfer data relative to the host CPU.

With specific reference to the exchange buffers 54, the preferred embodiment employs two FIFO registers 100, 102. The FIFO 100 receives data from the host CPU 30 via the adapter 20 and makes it available to the SPHSF 60. The FIFO 102 receives data from the SPHSF 60 and makes it available to the host

CPU 30 via the adapter 20. The dual port RAM 104 which allows both the host CPU 30 via the socket adapter 20 and/or the SPHSF 60 to read and write data autonomously and asynchronously in at random addresses. The dual port RAM provides substantial flexibility in the data exchange sequence. The SPHSF, for example, accesses stored data at random as needed, or can "look" at data in the RAM without deleting it. The host can, for example, enter and change commands in the RAM whether or not the SPHSF ever accesses or utilizes the them. The FIFOs are each one-way circuits, as their name implies, and whatever data goes in, comes out in the same order.

If the SPHSF is of the type including a programmable component such as a microprocessor, then the host CPU is adaptable to provide instruction codes to the programmable component via the data exchange circuitry. Specifically, the data exchange circuitry is operable to transfer not only operand data but instruction codes and commands, as well.

In order to make the transfer scheme functional when plugged into the math chip socket, the data exchange circuitry must be able to communicate with the host CPU 30. This can be accomplished by using one of the three following methods:

(1) The numerics chip may be plugged into the adapter, whereby the CPU 30 continues to communicate directly with the numerics chip and the data available at the adapter is lifted from the chip socket for use by the data exchange circuitry and the SPHSF;

(2) The math chip interface signal emulation logic circuitry 24 includes logic for duplicating

the protocol and accessing schemes of the numerics chip to simulate the identity of the numerics chip, permitting the host CPU 30 to function as if it were communicating directly with a standard numerics chip; or

(3) The data exchange circuitry can have a distinct identity provided that specific signals present in the math chip are handled in a manner compatible with the host CPU, i.e., the interface emulates the selected, required minimum protocol of the math chip while ignoring superfluous signals not relevant to the SPHSF.

An example for providing signal emulation is incorporated in the state machine shown in Fig. 3 which is the architecture for a typical state machine for the Intel 80386 microprocessor is illustrated in Fig. 3. The information for creating the state machine is directly available from the Intel 80386 Users Manual. The state machine logic is loaded into PLD circuits provided in the math chip CPU control logic circuitry 108. The math chip CPU control logic circuit communicates directly with the host CPU 30 through the math chip socket adapter 20 and emulates protocol and accessing schemes of a numerics chip, permitting the CPU 30 to function as if it were communicating with the numerics chip.

The math chip CPU control logic 108 communicates directly with the math chip socket to provide emulation. The address decoder is standard decoder architecture similar to that used in the numerics chip or other add-in function peripherals and provides the required handshaking signals between the peripheral and the host CPU 30.

The SPHSF 60 can be any special purpose high-speed functional peripheral. The SPHSF may include a CPU 120 which is adapted for receiving and sending data signals to and from the host CPU 30. In the prior art systems, the SPHSF would have to communicate directly with the host processor through the standard backplane. Where the SPHSF was capable of providing high-speed functions, the system efficiency was entirely dependent upon the speed of the backplane. By using the subject invention, the data exchange circuitry can receive data between the SPHSF 60 and the host CPU 30 at the speed it is generated and supply on demand, as needed. The peak data transfer rate is the data utilization rate of the SPHSF. The SPHSF interface logic circuit 56 in the data exchange circuitry would be customized for each specific SPHSF. The SPHSF may be expandable and adapted to include additional peripherals, as illustrated by DRAM control 122 and DRAM expansion board 124.

It will be readily appreciated that the use of the data transfer scheme of the present invention permits utilization of special purpose high-speed functional add-in peripherals with stand alone computer systems, wherein the rate of data transfer between the SPHSF and the host computer is limited only by the speed at which both the host processor and the add-in peripheral generate and utilize data, rather than being limited by standard backplane architecture. This permits the user to buy a relatively inexpensive PC or other microprocessor based host system and add to it the data transfer system of the present invention for substantially less investment than required to purchase a mini-computer or a mainframe, permitting performance levels at mini-computer or mainframe speeds. For example, using the invention with a PC having an Intel

386 microprocessor and an SPHSF includes an Intel 80860 microprocessor, numerical processing sequences can be performed at about half the rate of a CRAY-1 supercomputer at less than 1% of the cost.

A detailed schematic diagram of a data transfer interface device made in accordance with the present invention is illustrated in Figs. 4-13. As illustrated, the cable connectors provide direct access to the host CPU signals and to other useful signals which can be utilized to provide the optimum interface between the host and the add-in SPHSF. In Fig. 4, the upper PLD U1 implements a state machine which tracks the state machine of the host CPU (Fig. 3) by monitoring the signals available via the cable from the adapter. The upper PLD also implements the required handshaking signals according to the host CPU's required protocol for the transfer of data to and from the host. The lower PLD U2 implements the control signals used to interface with the data exchange buffers and other control logic.

In Fig. 5, the PLD U3 implements the control logic for the exchange of data from the host CPU's side of the data exchange buffers. In this case, they control reading from and writing to FIFO and random access dual port memories. The other side of the FIFOs and dual port memories is written to or read from by the SPHSF. The PAL U4 performs the same functions as the PAL U3 except that this PAL performs it's functions on behalf of the SPHSF, and thus is connected to the logically opposite side of the various buffers and control circuits.

In Fig. 6, the four cable connectors P4, P5, P6 and P7 carry the host CPU data bus signals to and from the host CPU socket adapter. In this design there are 32 host data bits, but if there were more or fewer

data bits, then the number of buffer logic chips would simply be adjusted to the required number to match the data bus width of the host CPU. The signals on the right side of Fig. 6 are the latched data bus bits from the host CPU or the unlatched data bus bits from the data exchange buffers.

The FIFO circuits in Fig. 7 comprise the lower 32 bits of the SPHSF data bus, which are also the even 32 bit words of the host CPU. These FIFOs pass data unidirectionally from the host to the SPHSF. The FIFO circuits in Fig. 8 comprise the upper 32 bits of the SPHSF data bus, which are also the odd 32 bit words of the host CPU. These FIFOs pass data unidirectionally from the host to the SPHSF. The FIFO circuits in Fig. 9 comprise the lower 32 bits of the SPHSF data bus, which are also the even 32 bit words of the host CPU. These FIFOs pass data unidirectionally from the SPHSF to the host. The FIFO circuits in Fig. 10 comprise the upper 32 bits of the SPHSF data bus, which are also the odd 32 bit words of the host CPU. These FIFOs pass data unidirectionally from the SPHSF to the host.

The dual port RAM chips U25 and U26 in Fig. 11, and U27 and U28 in Fig. 12 are each one megabit memories organized as 64K by 16 bits and are of the fully asynchronous dual ported variety. All signals on the left sides of the chips are connected to the host CPU and/or host interface control circuitry, and vise versa, all signals on the right side are connected to the SPHSF. This provides a random access memory for applications and algorithms not well suited for the sequential nature of FIFOs. The RAMs U25 and U26 from the lower 32 bits and the RAMs U27 and U28 from the upper 32 bits of the dual port RAM 104.

The dual port RAM chips U27 and U28 in Fig.

12 are each one megabit memories organized as 64K by 16 bits and are of the fully asynchronous dual ported variety. All signals on the left sides of the chips are connected to the host CPU and/or host interface control circuitry, and vice versa, all signals on the right side are connected to the SPHSF unit. This provides a random access memory for applications and algorithms not well suited for the sequential nature of FIFOs.

The SPHSF shown in Fig. 13 is shown merely as an example and is a 64 bit high speed RISC processor which is to be used primarily as an accelerator for numerical computation intensive applications. The high speed interface to the host could be utilized for virtually any special function which would benefit from high data transfer rates. Examples would be mass storage controllers, signal processing sub-systems, image processors and the like.

While certain features and embodiments of the invention have been described herein, it will be understood that the invention includes all alternatives encompassed within the scope and spirit of the following claims.

CLAIMS

What is claimed is:

1. A host/peripheral interface for providing the transfer of data between a host processor and a remote special purpose high-speed system, the transfer means comprising:

a. an adapter for connecting said interface directly to a data access point associated directly with the host processor;

b. logic means in communication with the adapter for establishing protocol and access schemes acceptable to the host processor for signaling the host processor to send and receive data at the data access point; and

c. a data transfer device in direct communication with the adapter and the remote system for transmitting data between the host processor and the remote system at a data transfer rate equal to the rate said data is generated by the respective host processor and/or remote system.

2. The host/peripheral interface of Claim 1, the data transfer device further comprising:

a. a first buffer means in communication with the adapter and the remote system for receiving data generated by the host processor and for storing the data for release to or use by the remote system on an as-needed basis; and

b. a second buffer means in communication with the remote system and the adapter for receiving data generated by the remote system and for storing the data for release to or use by the host processor; and

3. The host/peripheral interface of Claim 2, further including a data exchange logic device in communication with the adapter, the remote system and the buffer means for signaling to each buffer means

when the remote system is ready to use or receive the data stored in the respective buffer means.

4. The host/peripheral interface of Claim 2, wherein each buffer means further comprises:

a. a first-in, first-out data storage device; and

b. a dual port memory in communication with the adapter and the host processor and the remote system.

5. The host/peripheral interface of Claim 4, each first-in, first-out register having a 512x64 configuration.

6. The host/peripheral interface of Claim 3, the host of the type generating control signals separate and distinct from the data signals, the data exchange logic device further comprising a control logic means for receiving the control signals and transmitting said control signals to the respective buffer means.

7. The host/peripheral interface of Claim 1, the host processor of the type including a standard extended math chip socket, the adapter further including means for connecting said interface device directly into said extended math chip socket.

8. The host/peripheral interface of Claim 7, the extended math chip socket connecting means further including means for connecting a numerics chip in the extended math chip socket in parallel with said host/peripheral interface device.

9. The host/peripheral interface of Claim 7, the logic means further including means for emulating the protocol and accessing schemes of a standard numerics chip.

10. A method for bypassing the backplane of a host processor when transmitting data between the host

processor and a remote special purpose high-speed add-in system, comprising the steps of:

a. selecting a data access point on the host processor;

b. emulating the protocol and access schemes required for the host processor to send and receive data to the access point;

c. collecting and storing data generated and transmitted by the host processor and the remote system; and

d. using the stored data.

11. The method according to Claim 10, the host processor of the type including an extended math chip socket, wherein the signals generated and transmitted by the host processor are collected at said socket, and wherein the signals generated and transmitted by the remote system are transmitted to said socket.

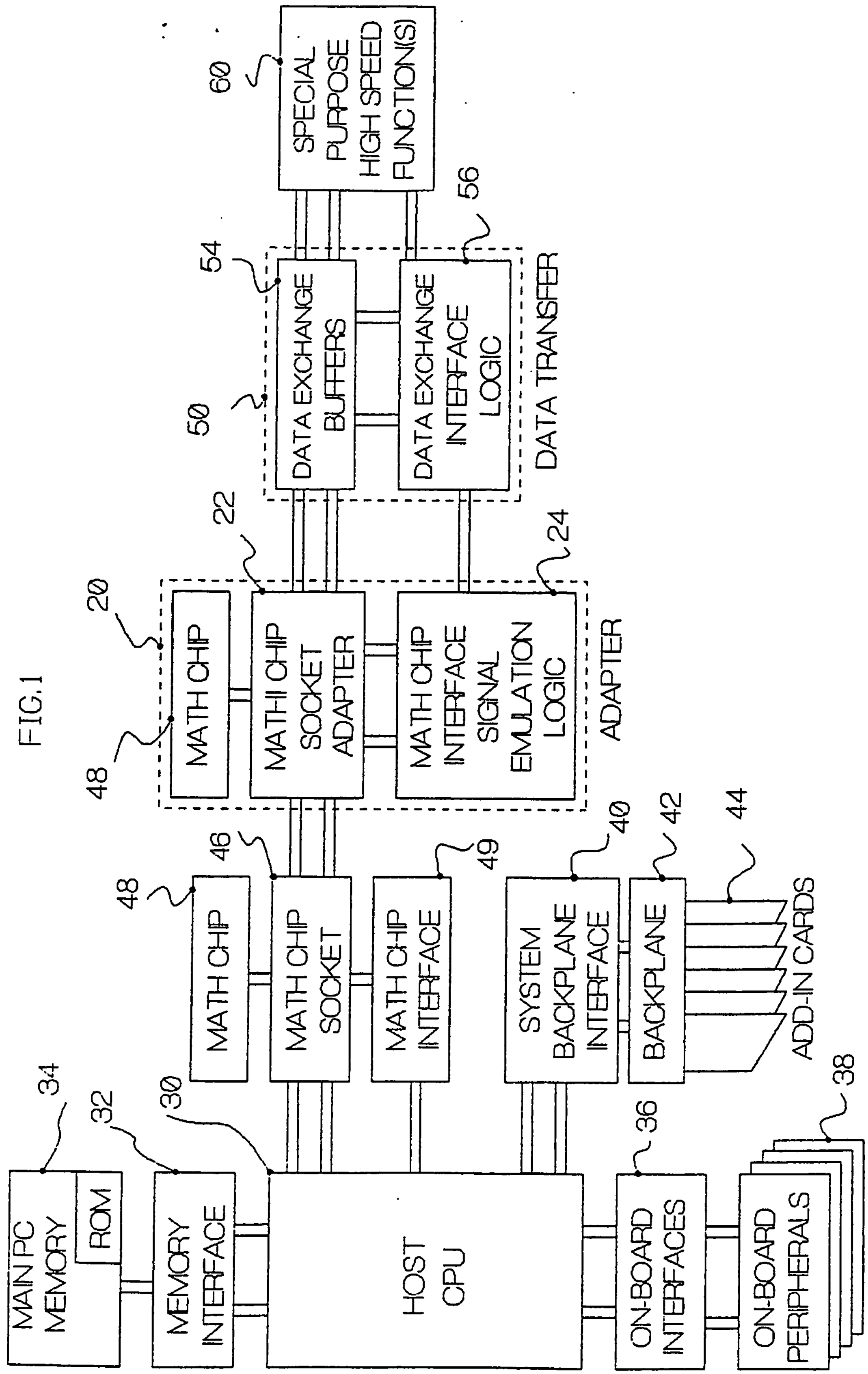

MAIN PC MEMORY
ROM
MEMORY INTERFACE
HOST CPU
ON-BOARD INTERFACES
ON-BOARD PERIPHERALS
MATH CHIP
MATH CHIP SOCKET
MATH CHIP INTERFACE
SYSTEM BACKPLANE INTERFACE
BACKPLANE
ADD-IN CARDS
MATH CHIP
MATHI CHIP SOCKET ADAPTER
MATH CHIP INTERFACE SIGNAL EMULATION LOGIC
ADAPTER
DATA EXCHANGE BUFFERS
DATA EXCHANGE INTERFACE LOGIC
DATA TRANSFER
SPECIAL PURPOSE HIGH SPEED FUNCTION(S)
20
22
24
30
32
34
36
38
40
42
44
46
48
48
49
50
54
56
60

FIG.1

FIG.2

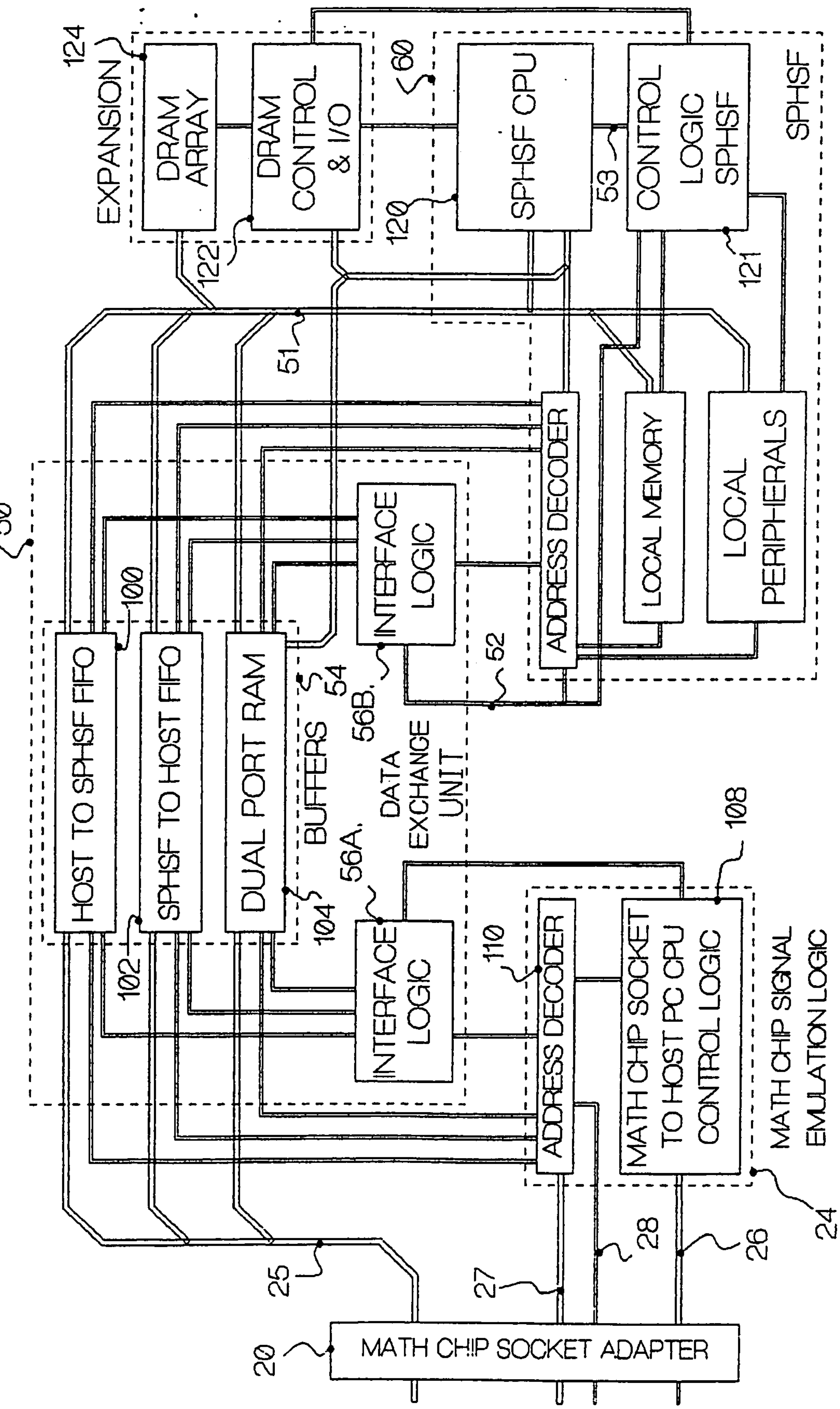
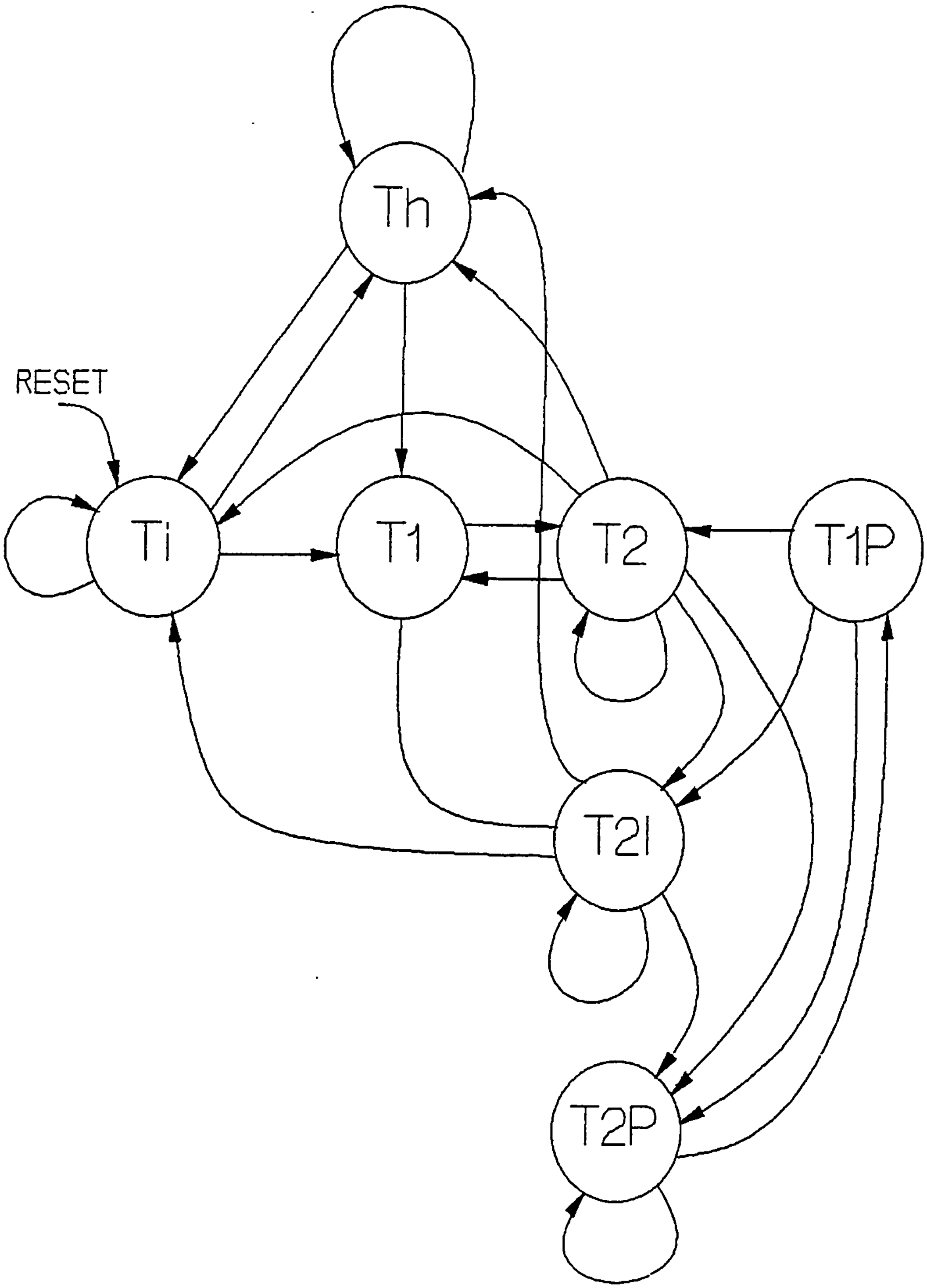
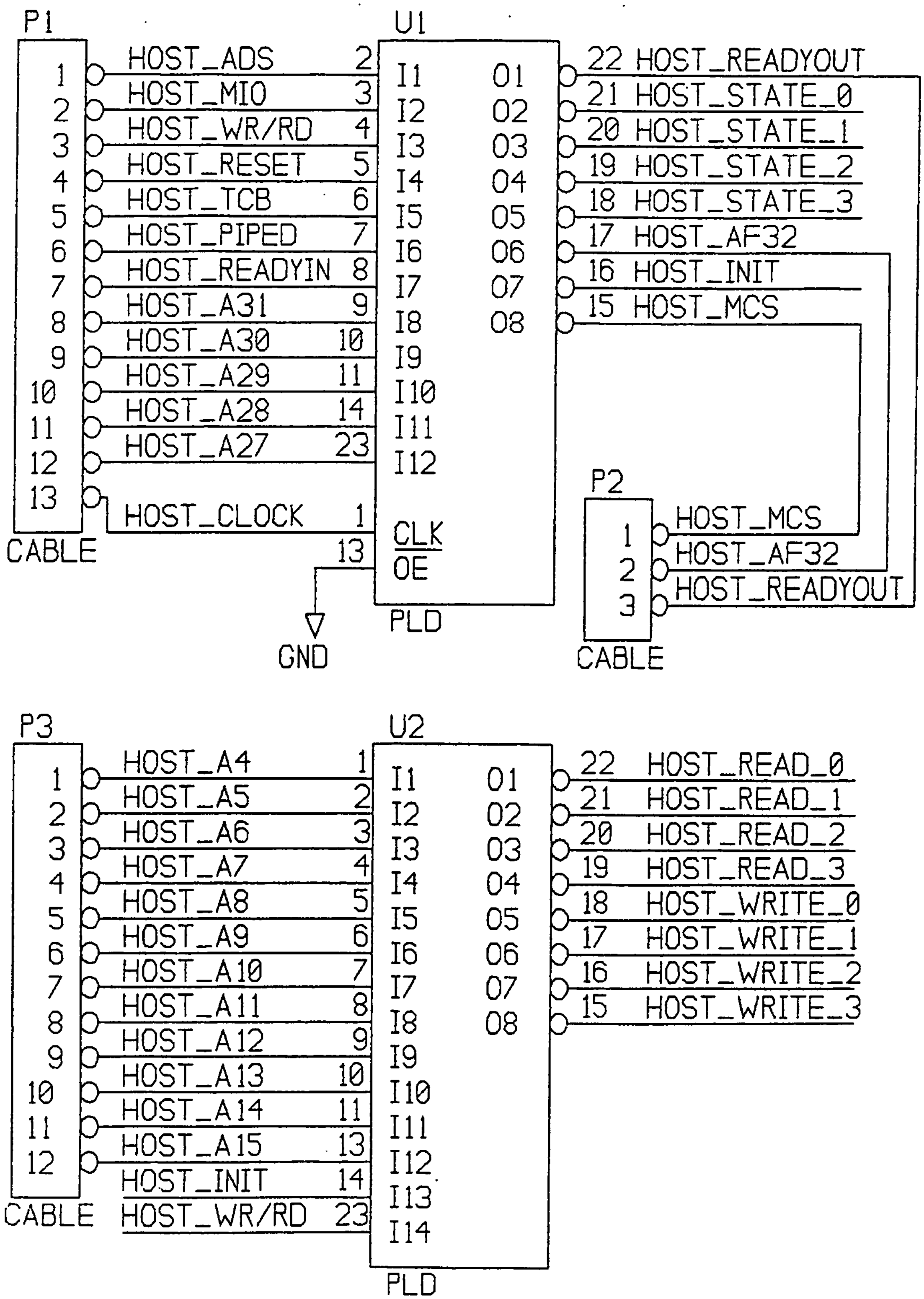

EXPANSION
DRAM ARRAY
DRAM CONTROL & I/O
124
122
60
SPHSF CPU
120
53
CONTROL LOGIC SPHSF
121
SPHSF
51
ADDRESS DECODER
LOCAL MEMORY
LOCAL PERIPHERALS
50
INTERFACE LOGIC
100
HOST TO SPHSF FIFO
SPHSF TO HOST FIFO
DUAL PORT RAM
54
56B
52
BUFFERS
DATA EXCHANGE UNIT
56A
104
102
INTERFACE LOGIC
110
ADDRESS DECODER
108
MATH CHIP SOCKET TO HOST PC CPU CONTROL LOGIC
MATH CHIP SIGNAL EMULATION LOGIC
24
25
27
28
26
20
MATH CHIP SOCKET ADAPTER

FIG.3
PRIOR ART



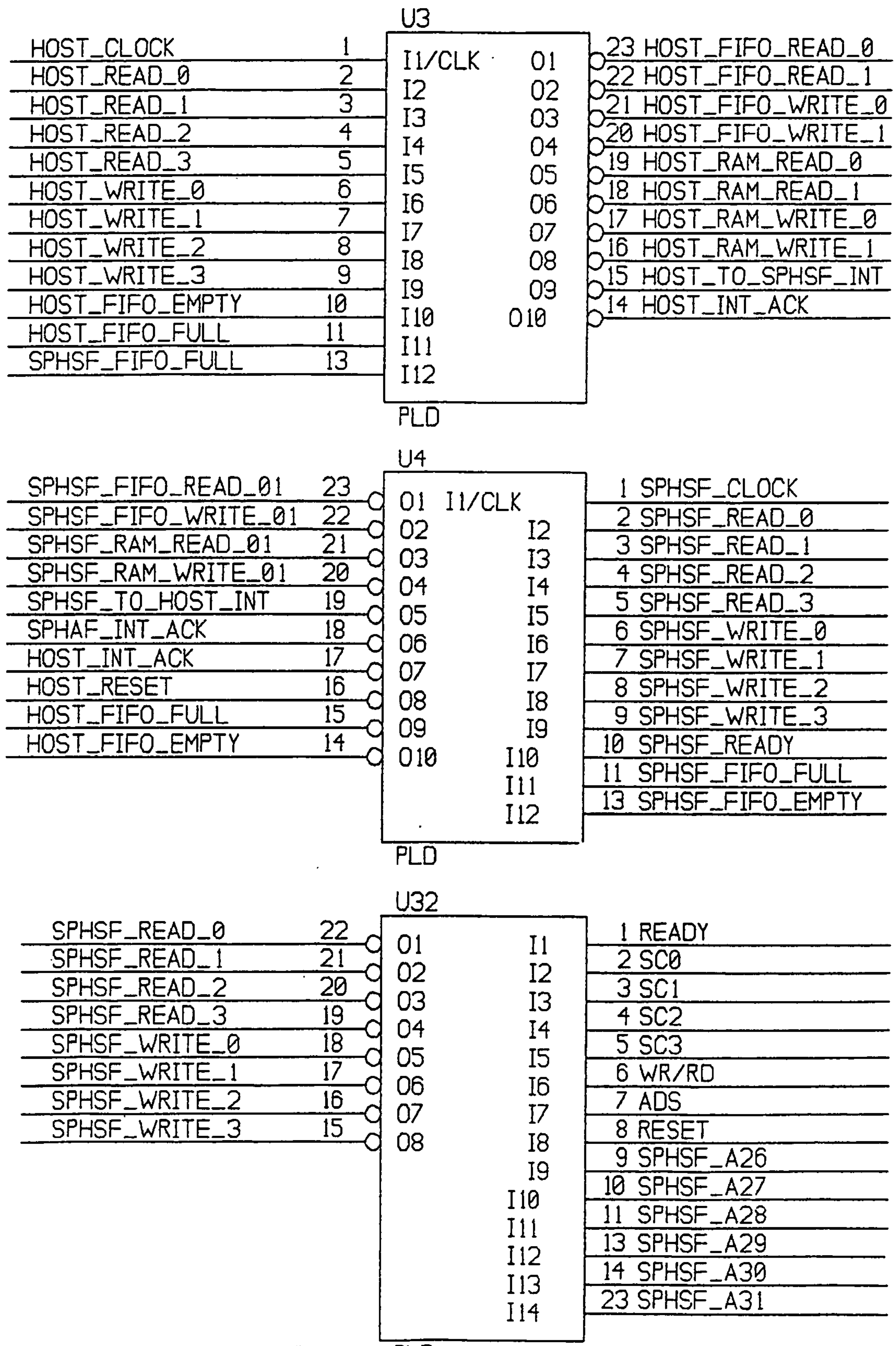
386 DX COMPLETE BUS STATES
(INCLUDING PIPELINED ADDRESS)

FIG.4



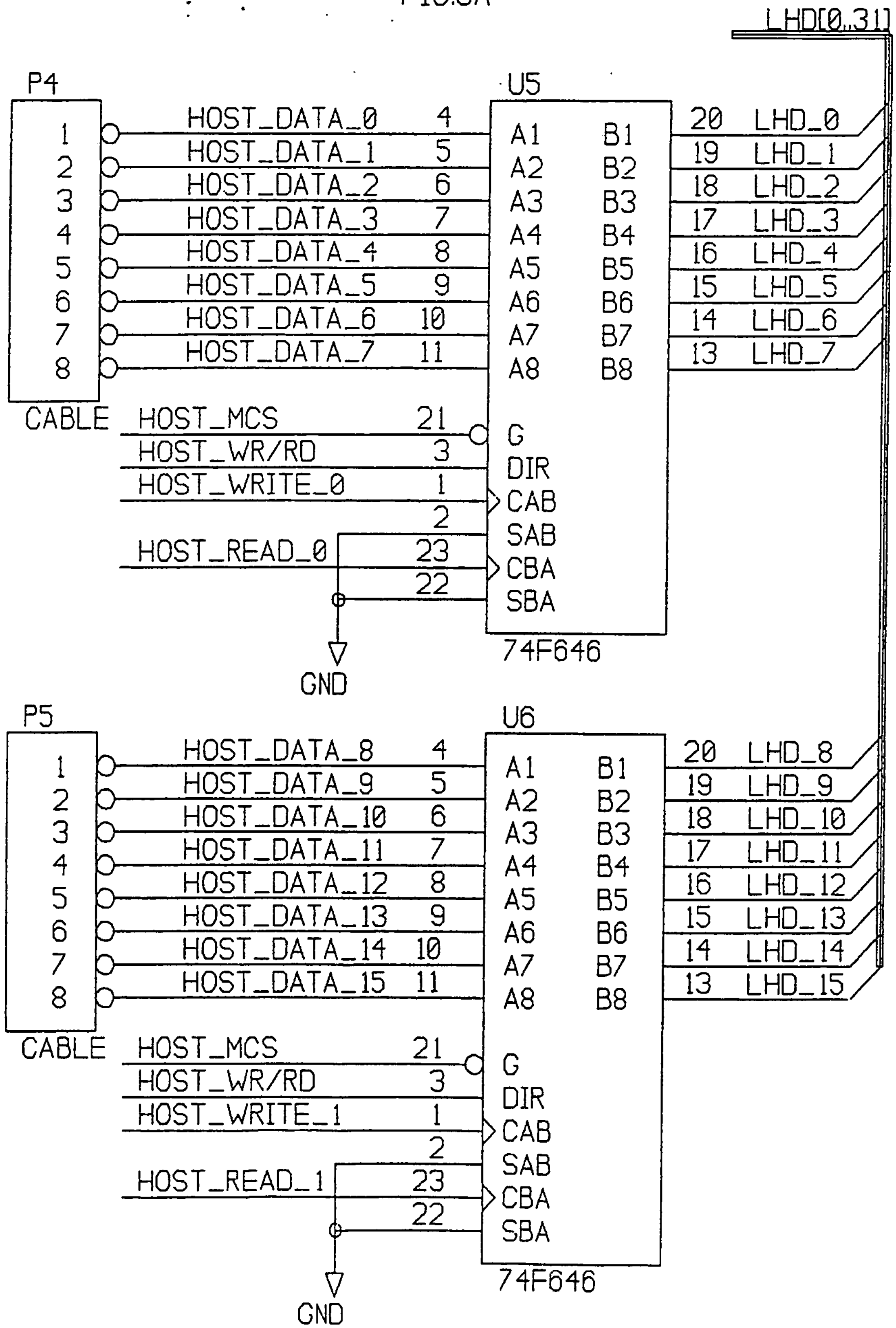
HOST I/O CONTROL LOGIC

FIG.5



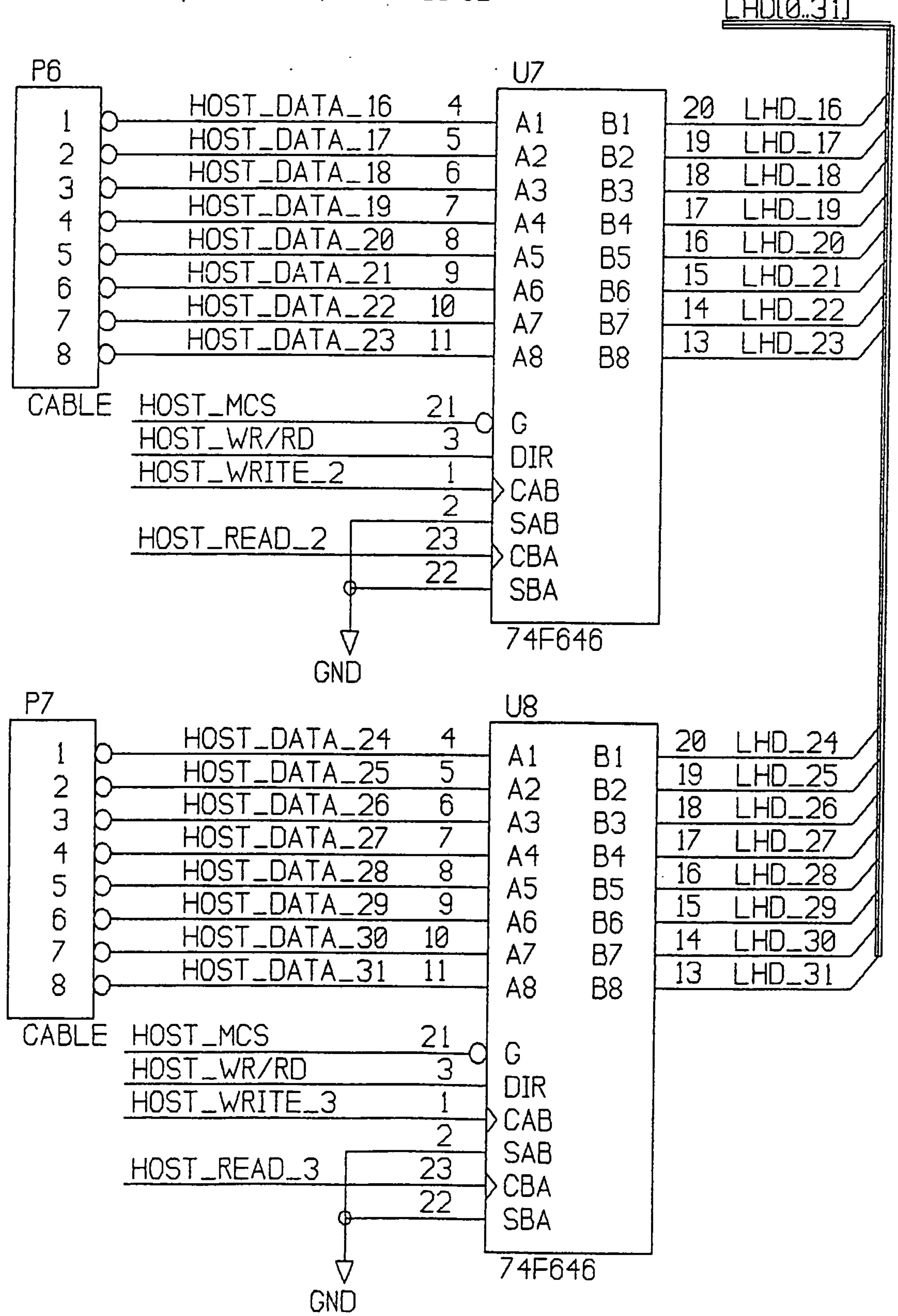
DATA EXCHANGE LOGIC

FIG.6A



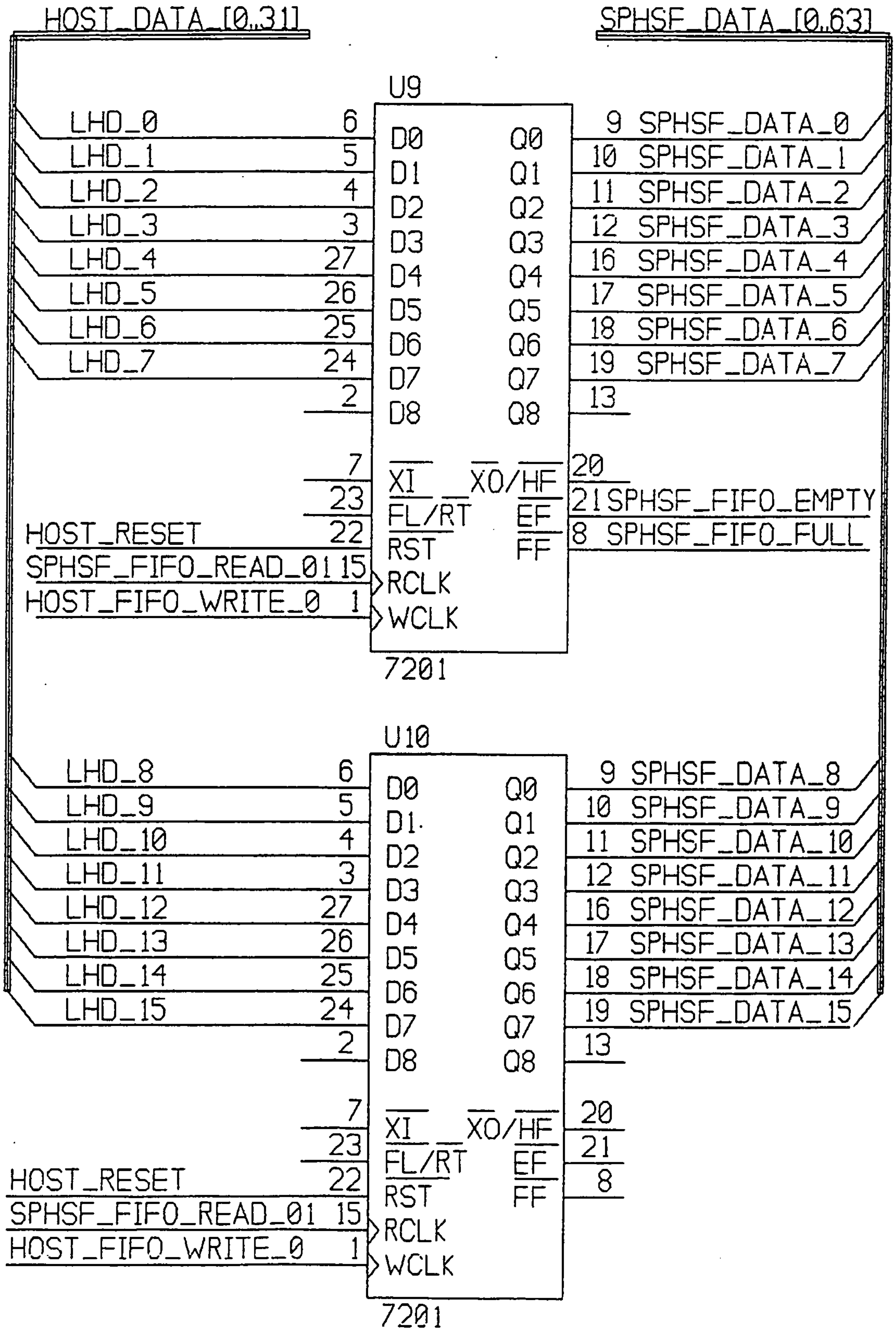
HOST DATA EXCHANGE REGISTERS

FIG.6B



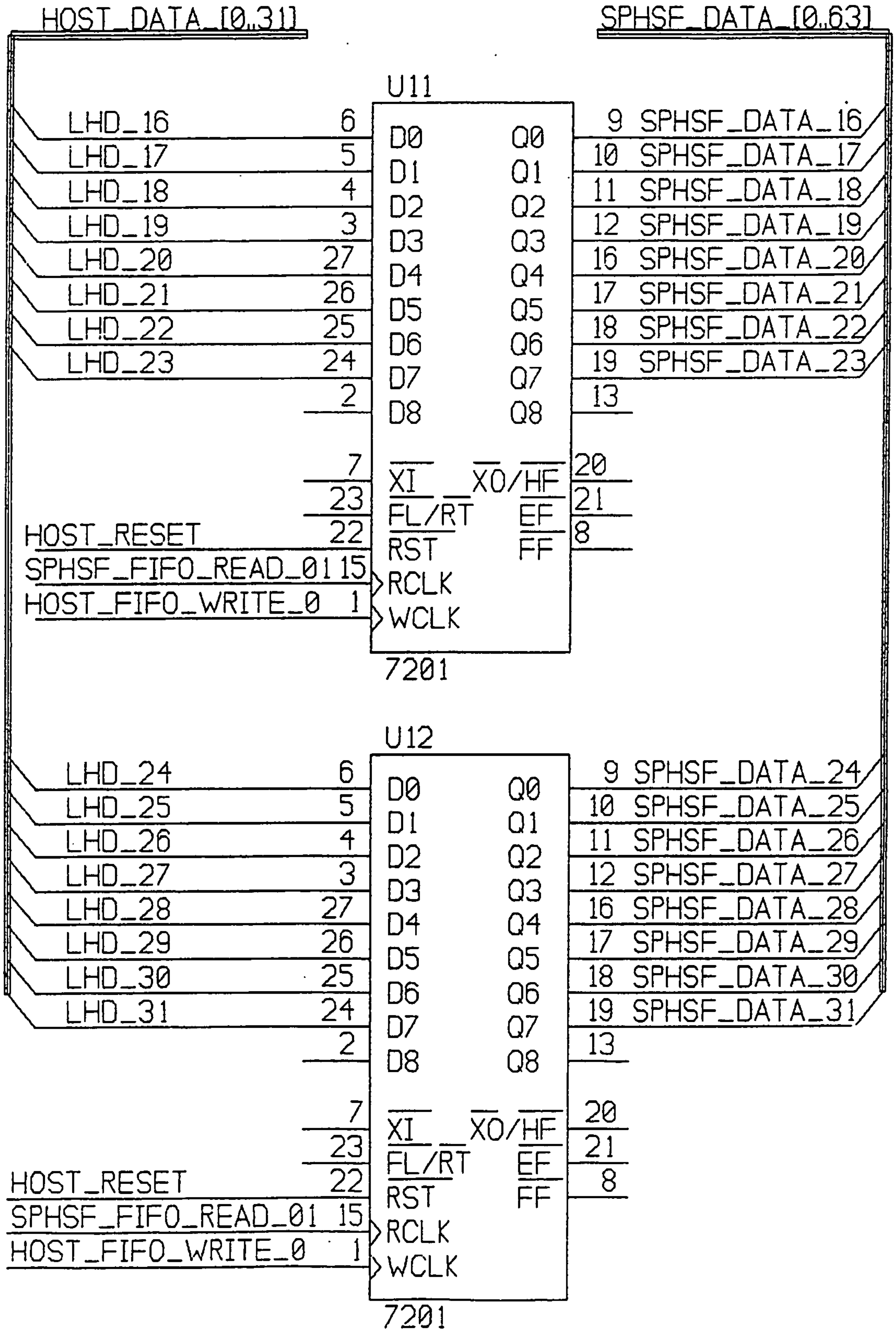
HOST DATA EXCHANGE REGISTERS

FIG.7A



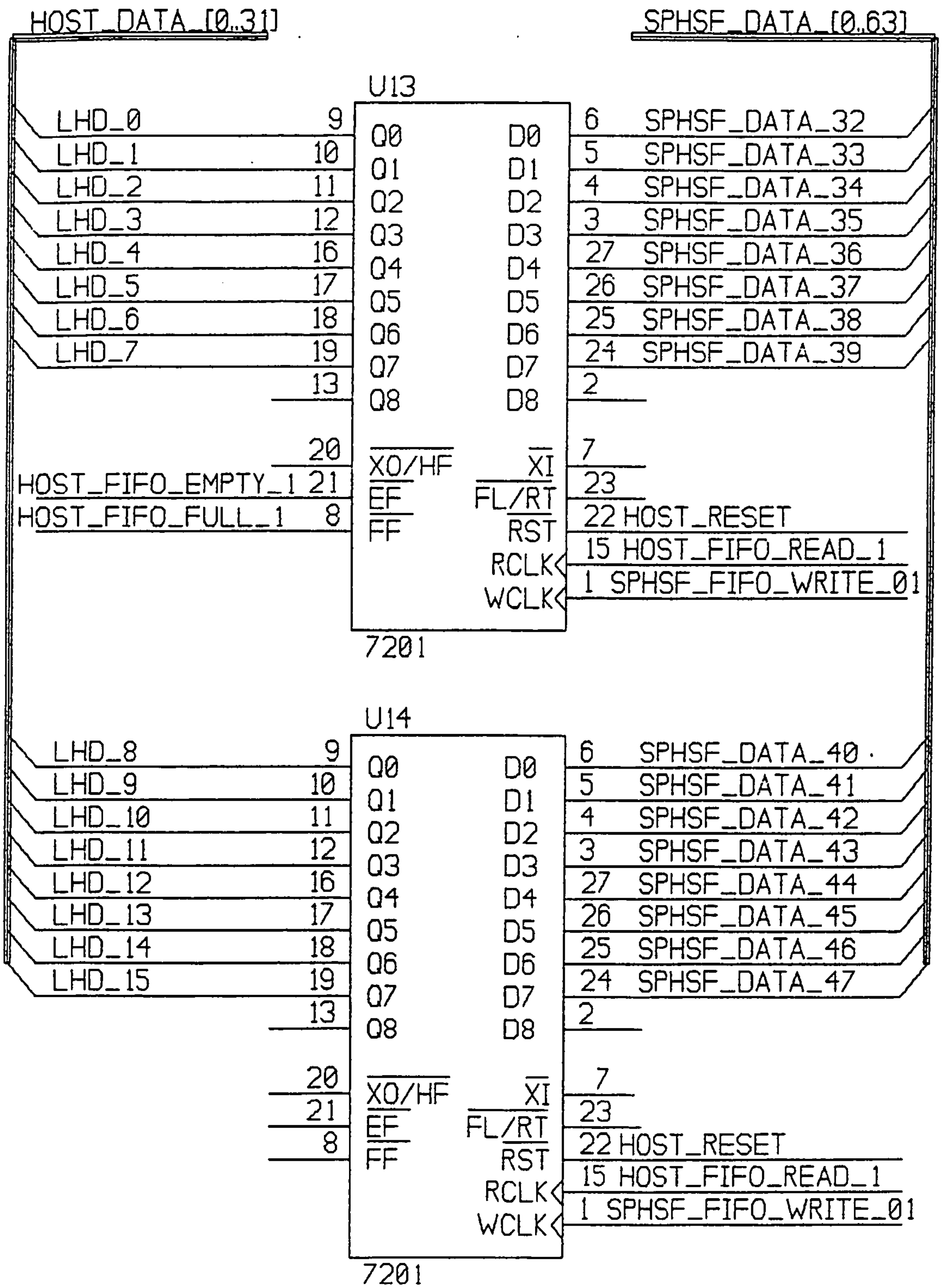
HOST TO SPHSF FIFO BITS 0 TO 15

FIG.7B



HOST TO SPHSF FIFO BITS 16 TO 31

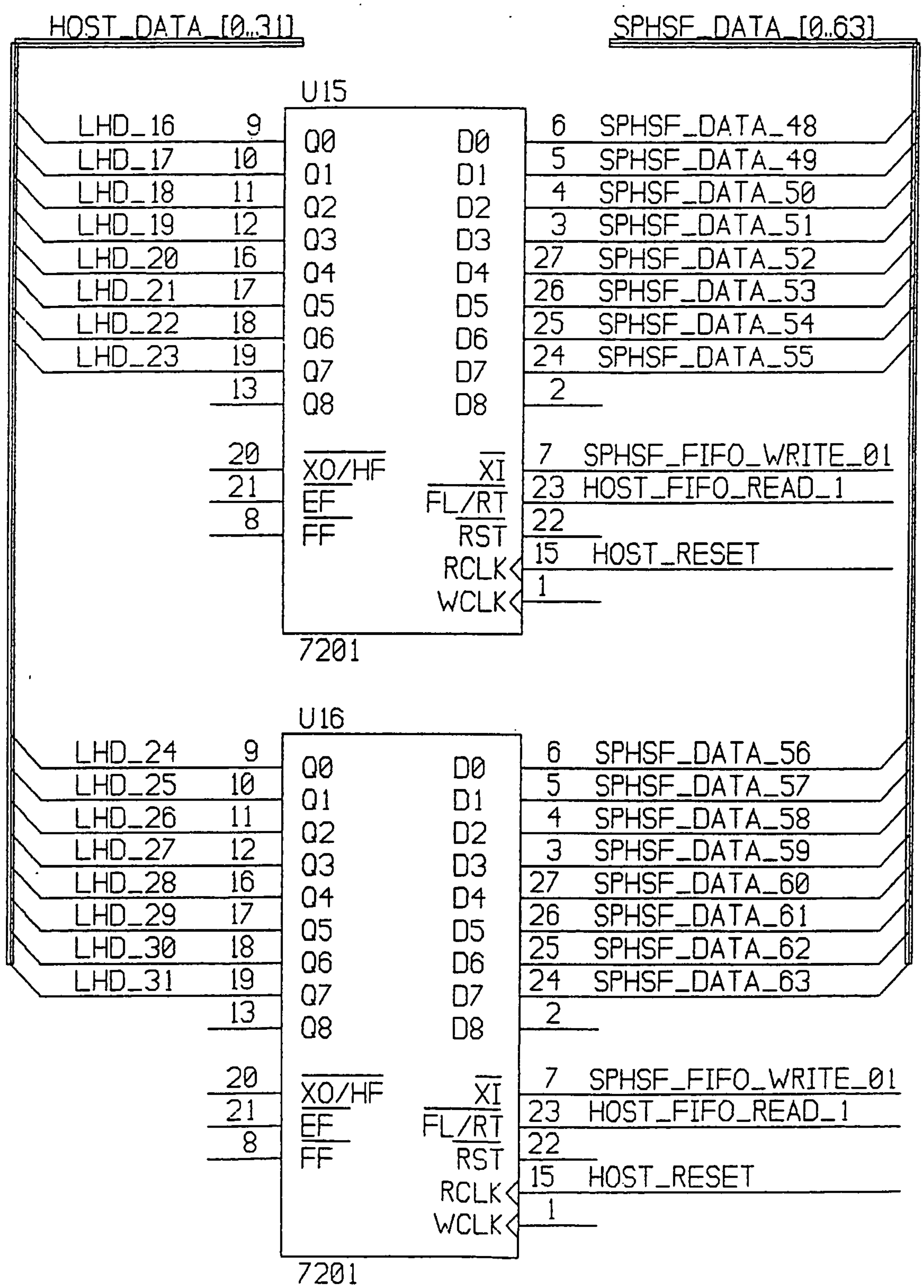
FIG.8A



SPHSF TO HOST FIFO BITS 32 TO 47

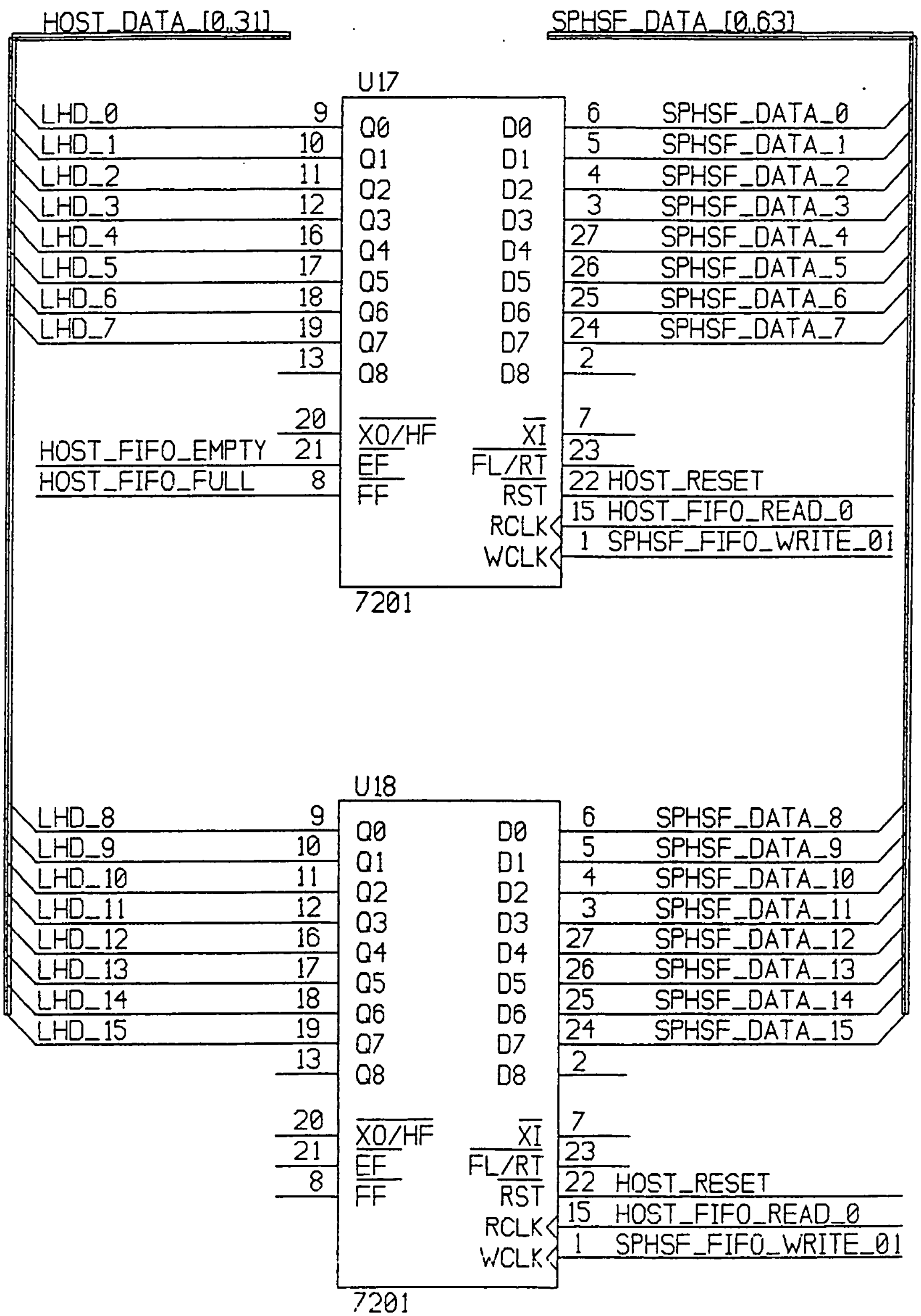
SUBSTITUTE SHEET

FIG.8B



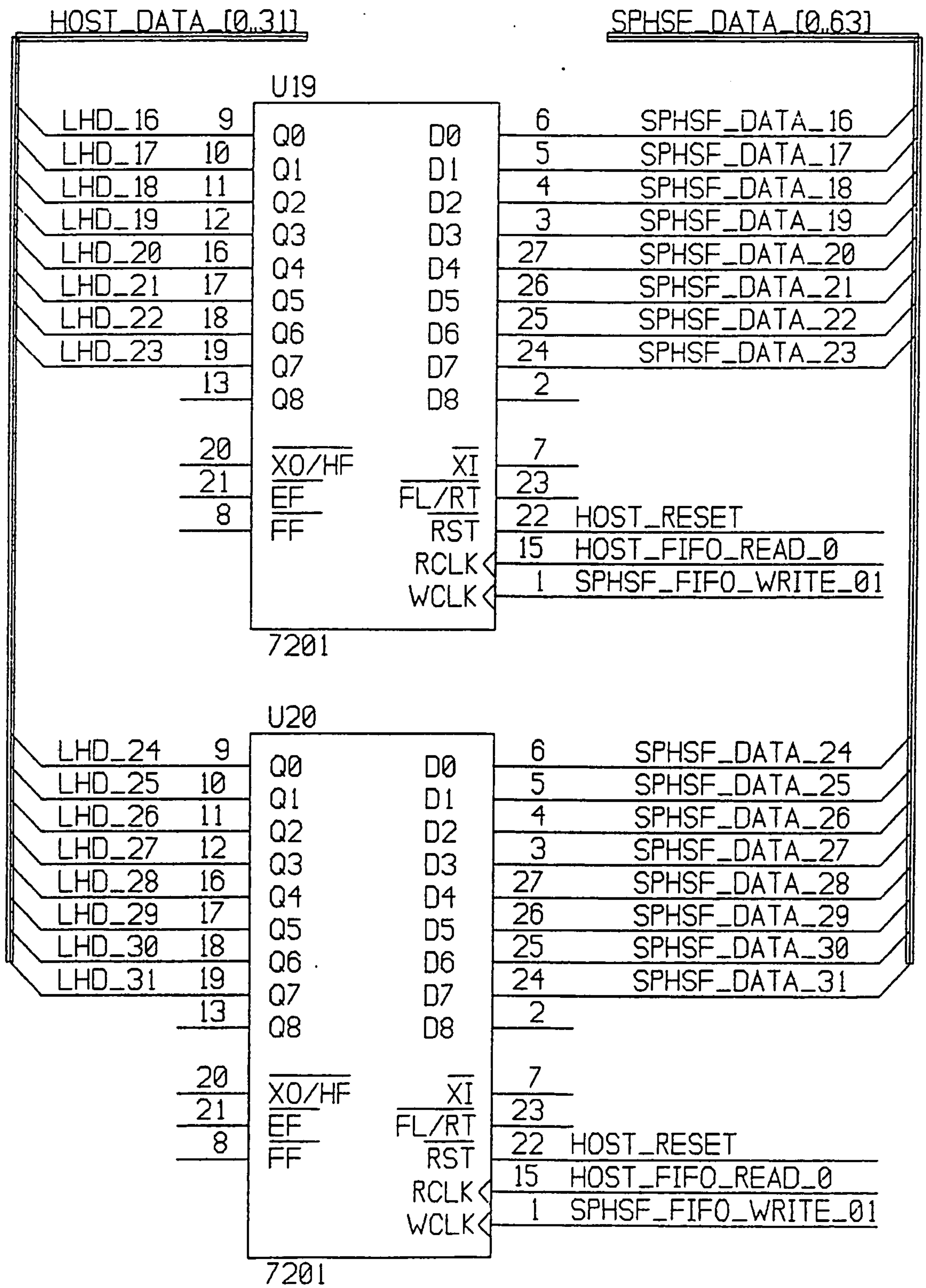
SPHSF TO HOST FIFO BITS 48 TO 63

FIG.9A



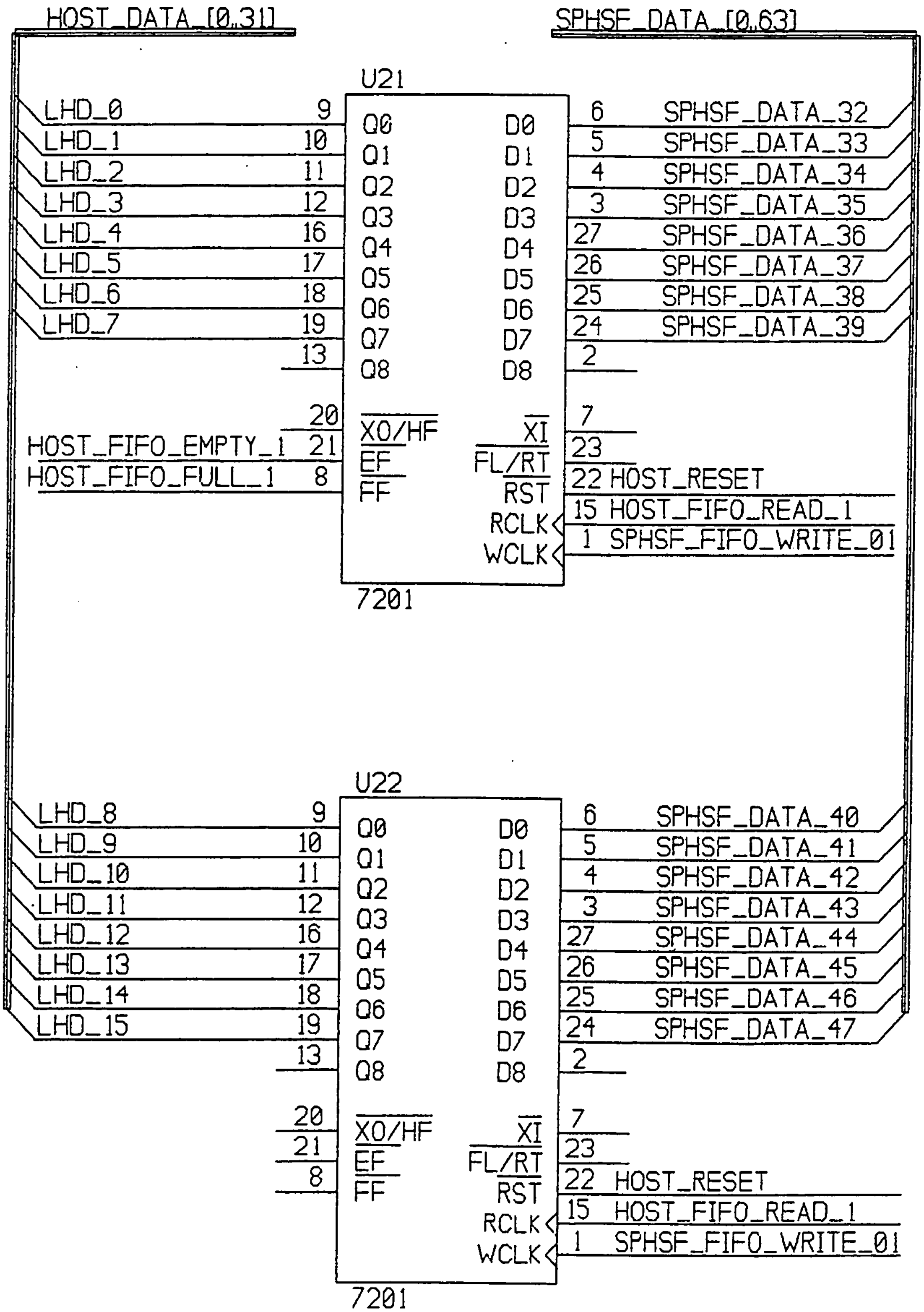
SPHSF TO HOST FIFO LOWER BITS 0 TO 15

FIG.9B



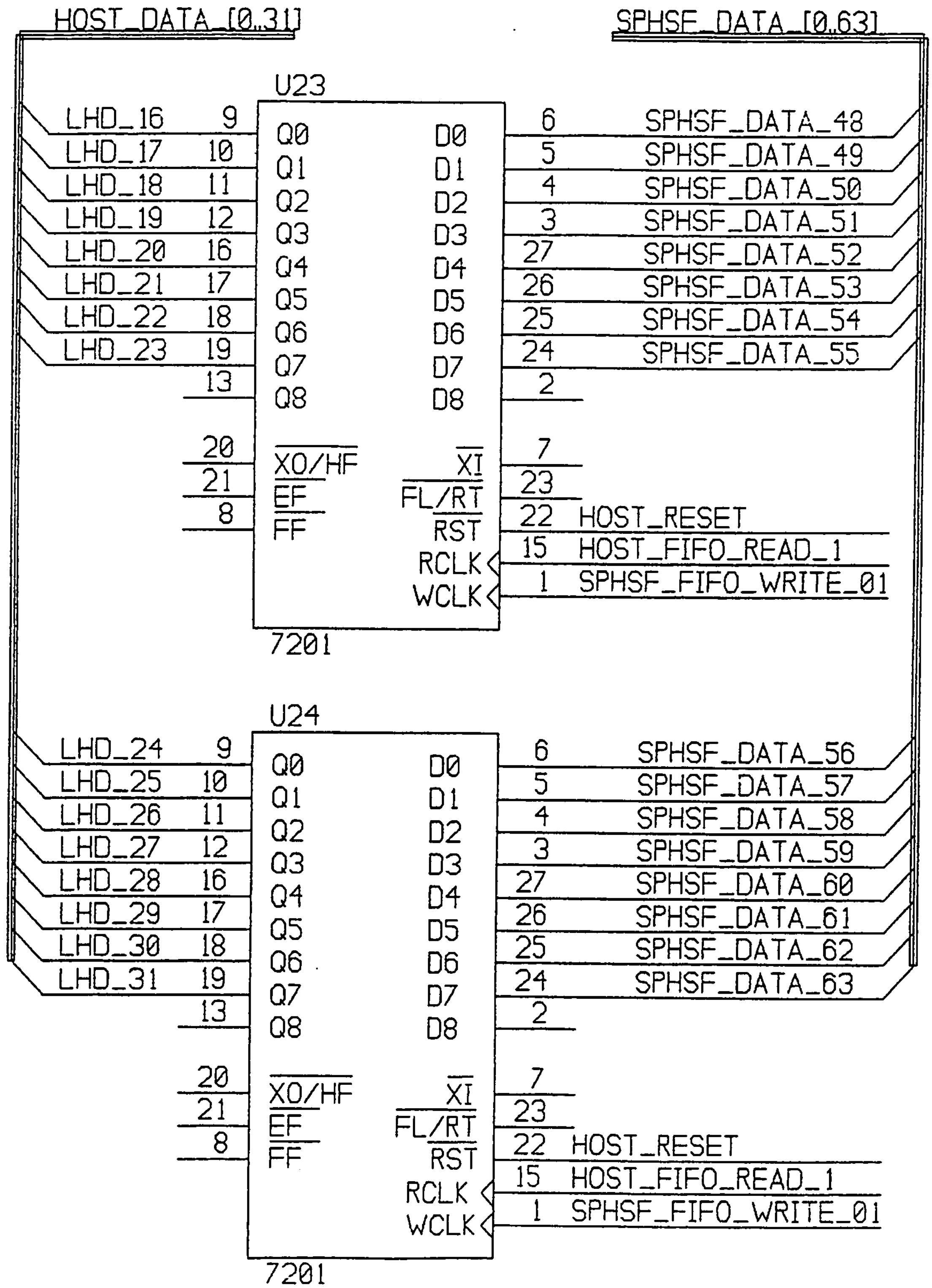
SPHSF TO HOST FIFO LOWER BITS 16 TO 31

FIG.10A



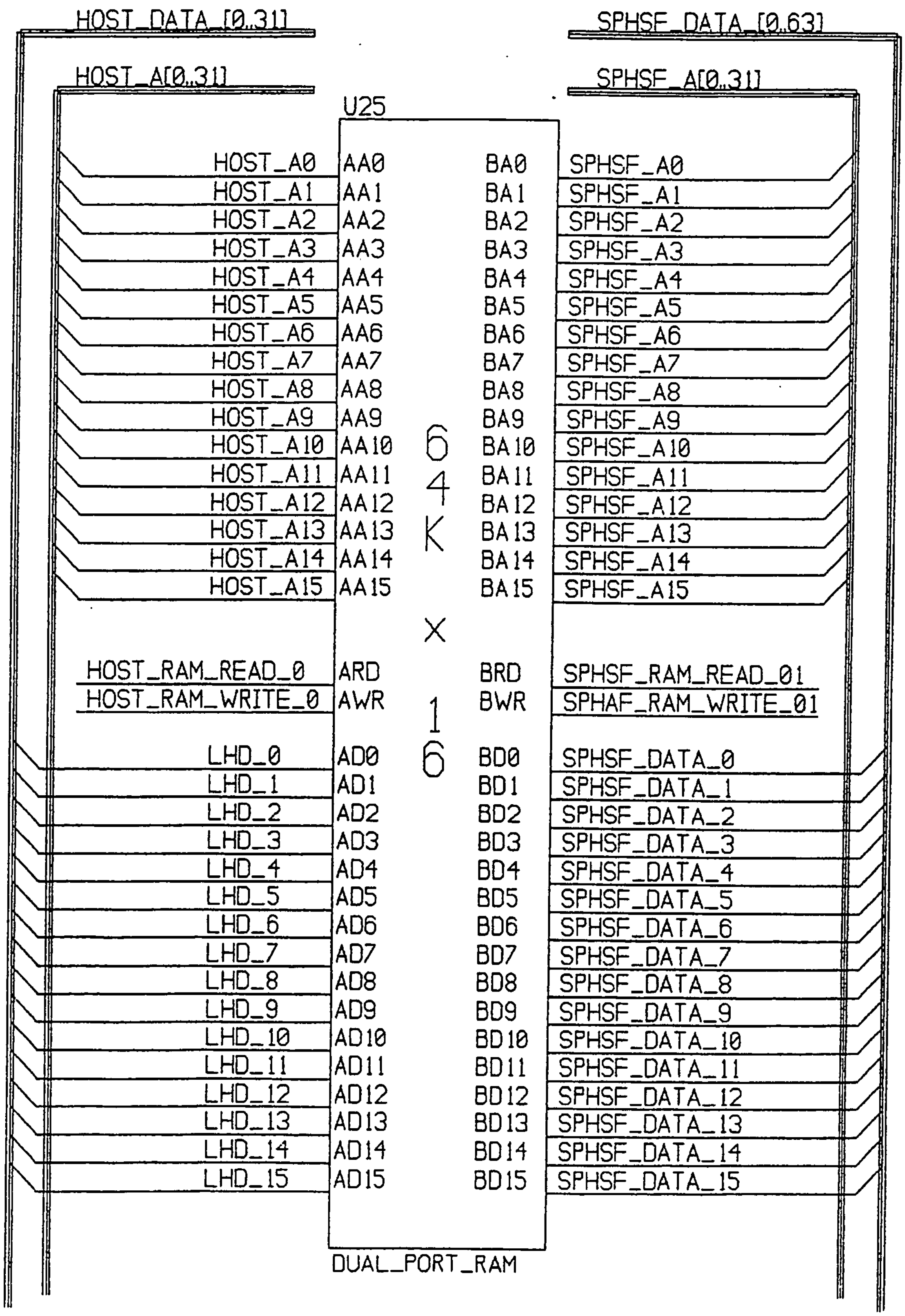
SPHSF TO HOST FIFO BITS 32 TO 47

FIG.10B



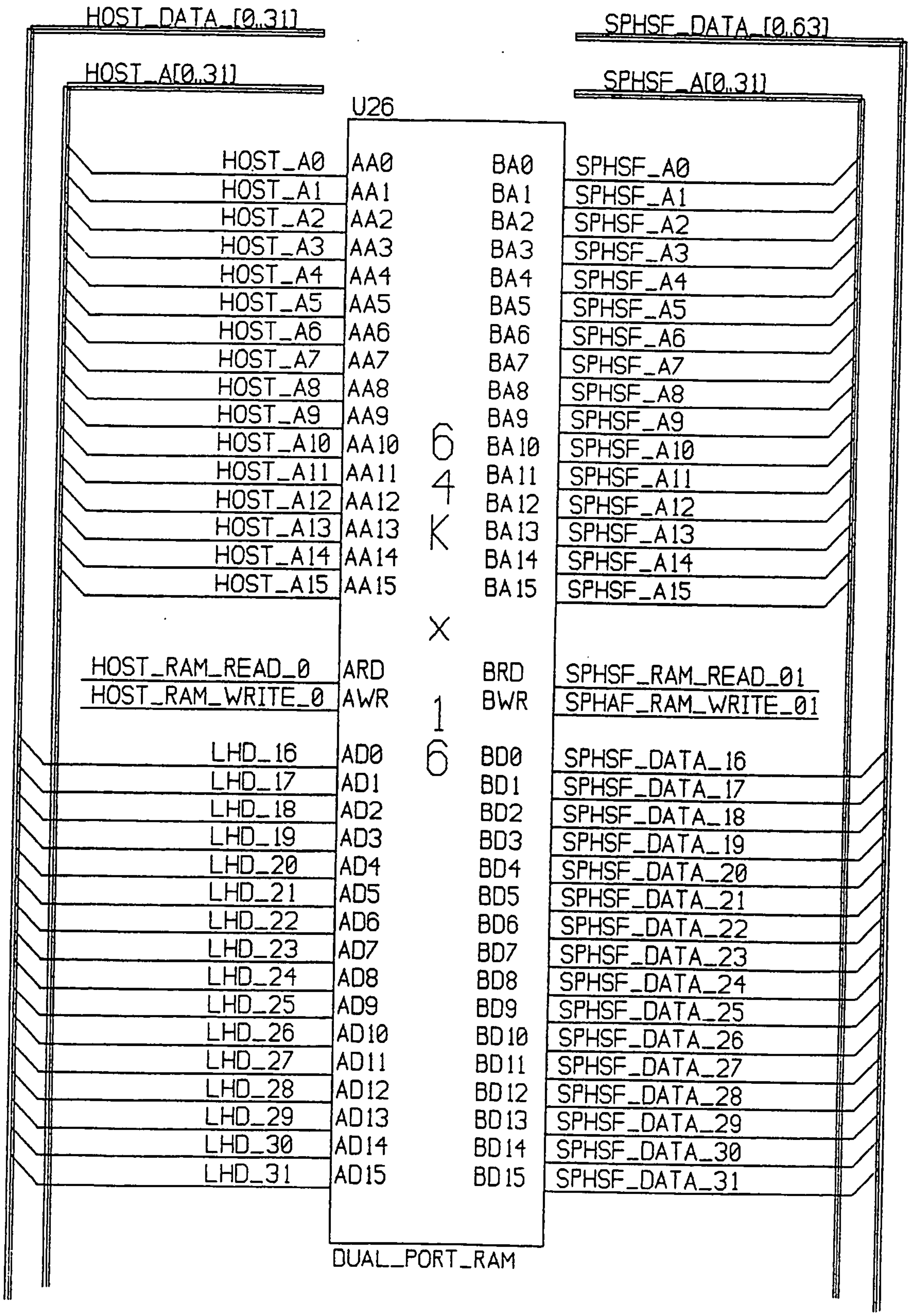
SPHSF TO HOST FIFO BITS 48 TO 63

FIG.11A



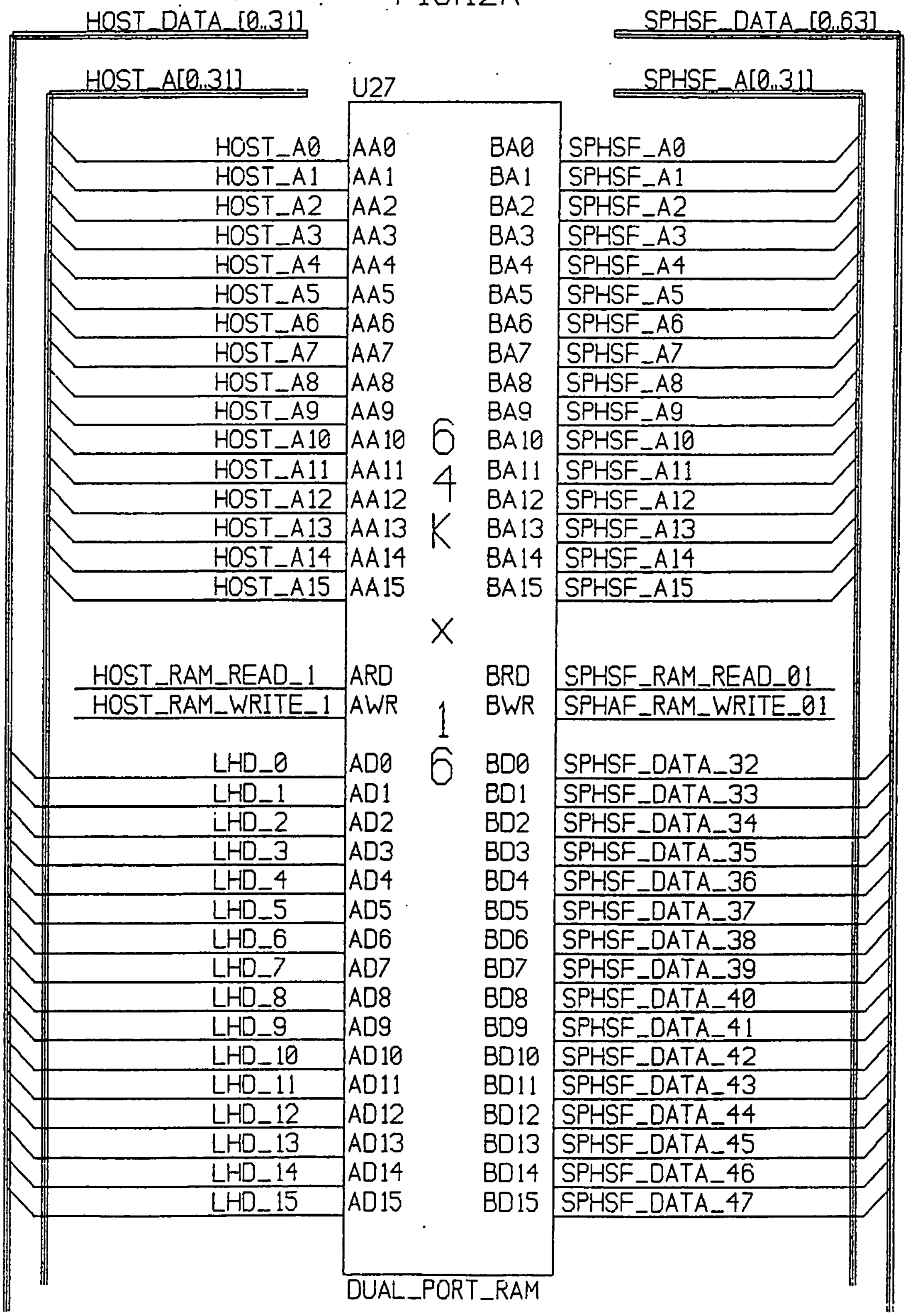
DUAL PORT RAM BITS 0 TO 15

FIG. 11B



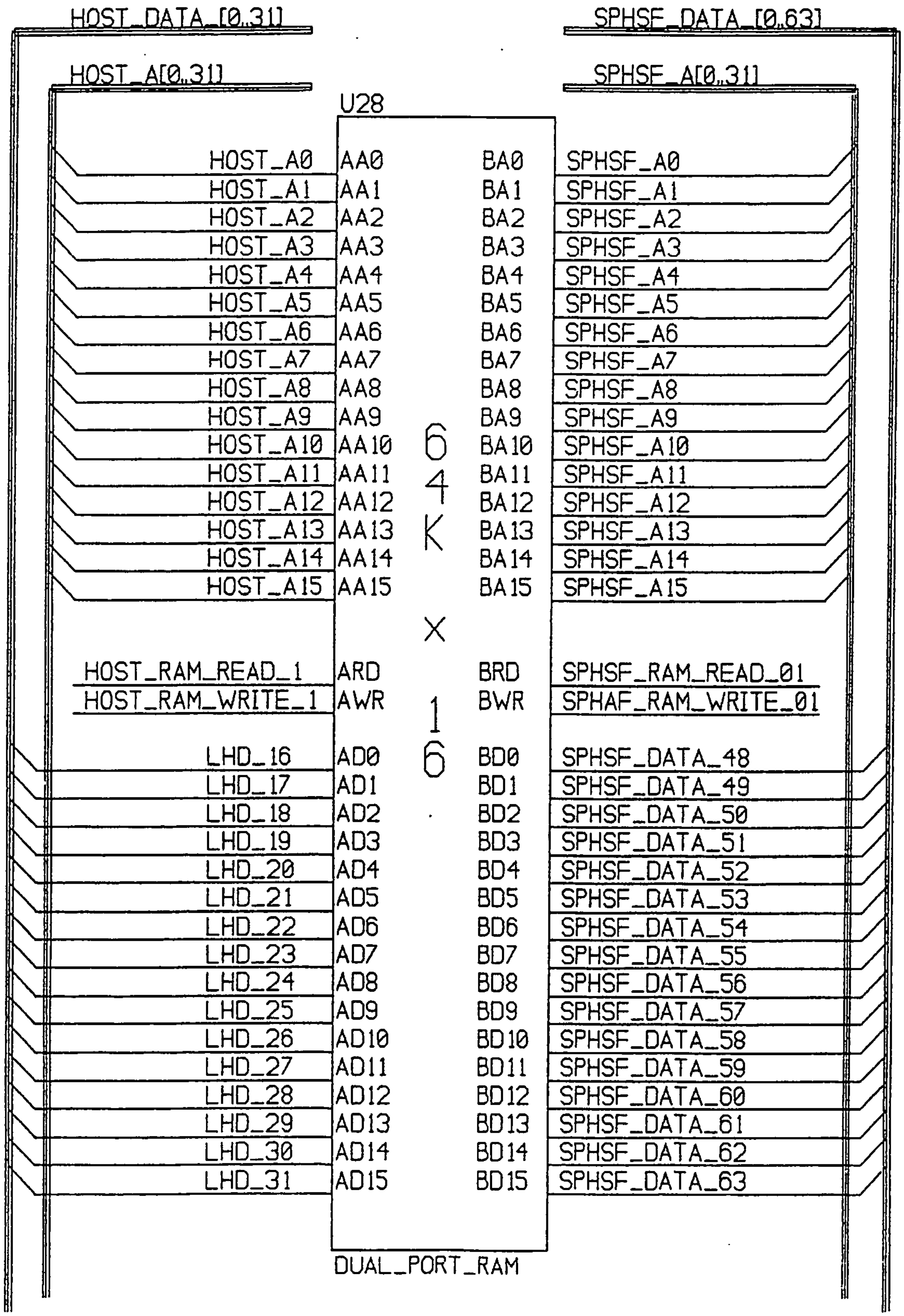
DUAL PORT RAM BITS 16 TO 31

FIG.12A



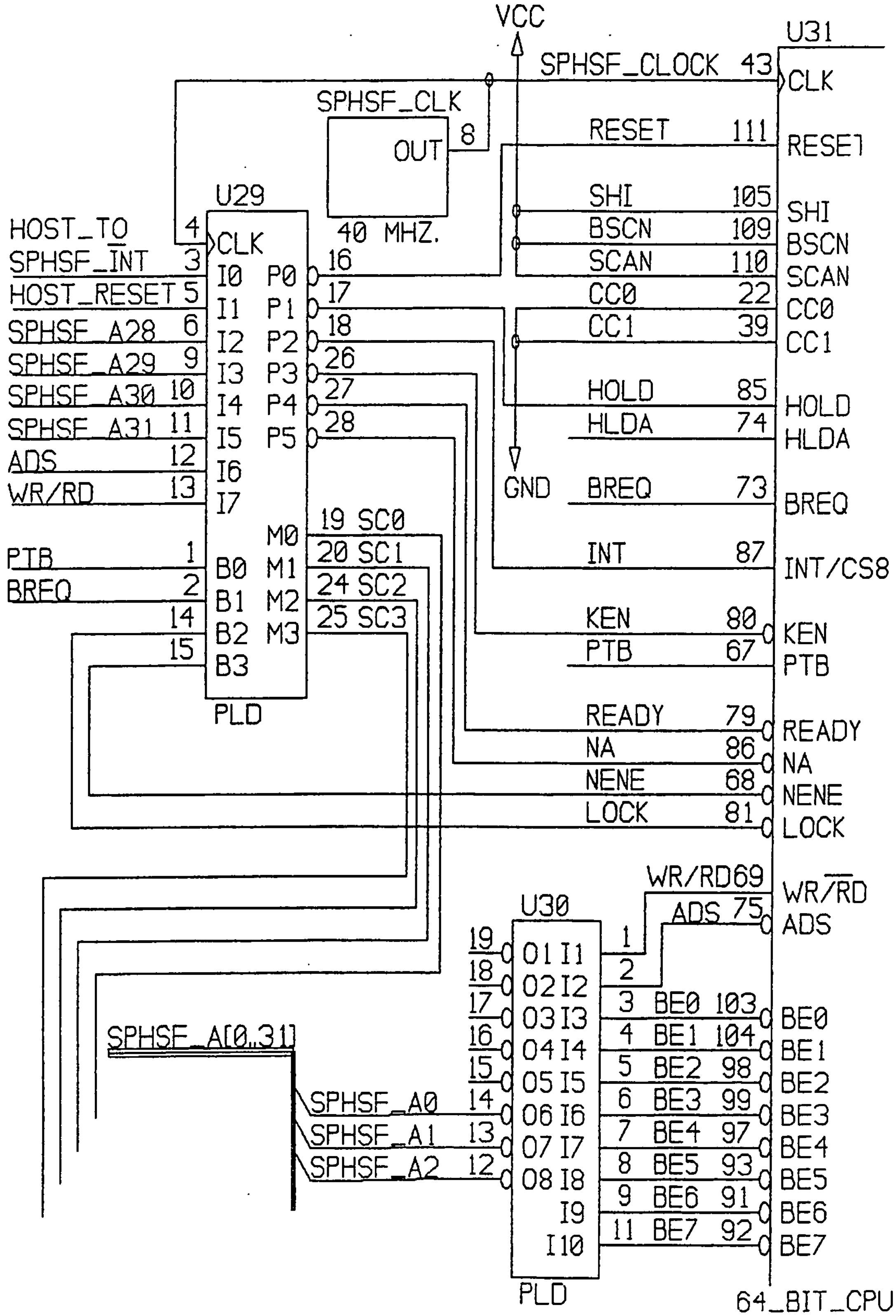
DUAL PORT RAM BITS 32 TO 47

FIG.12B



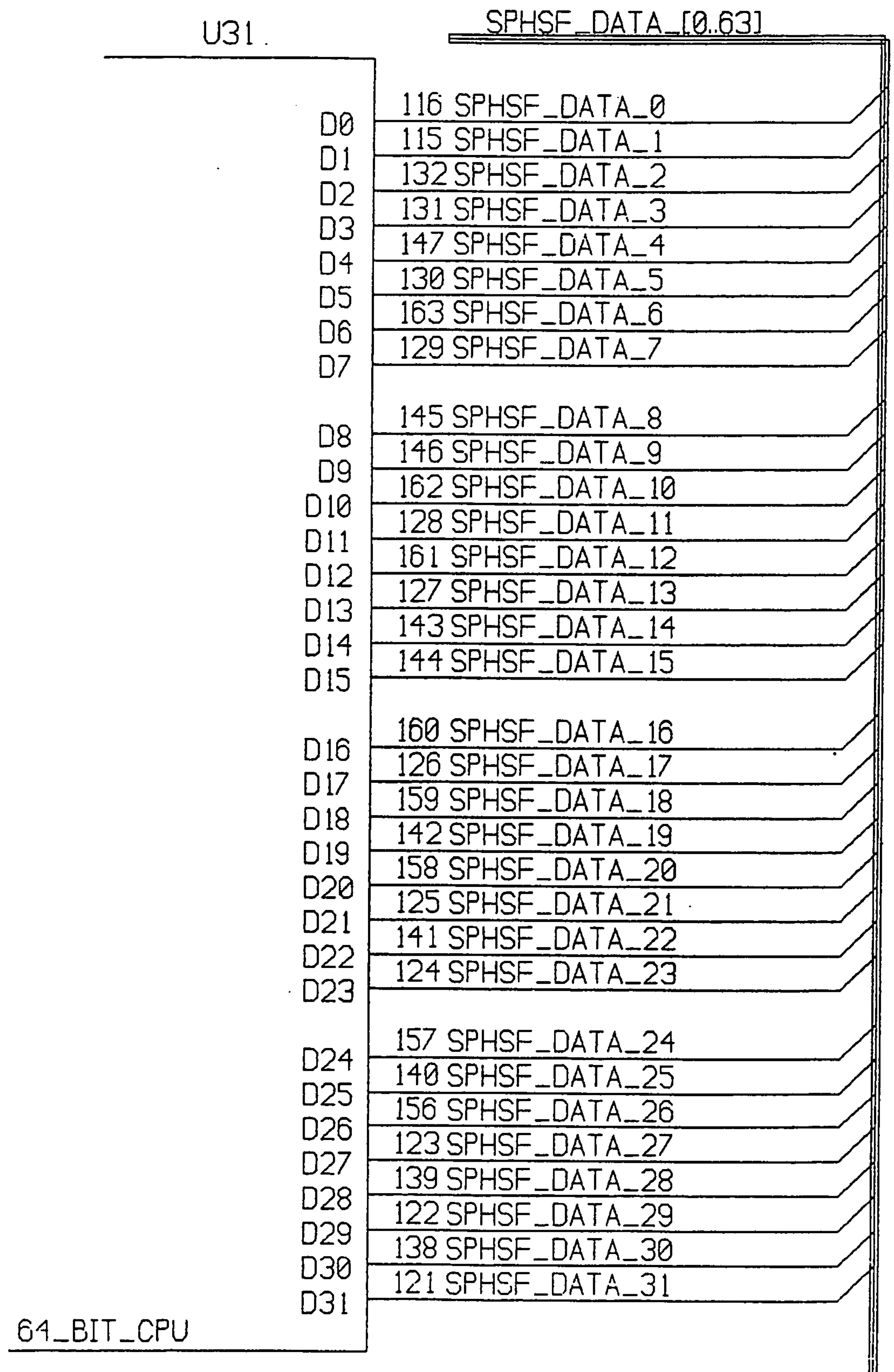
DUAL PORT RAM BITS 48 TO 63

FIG.13A



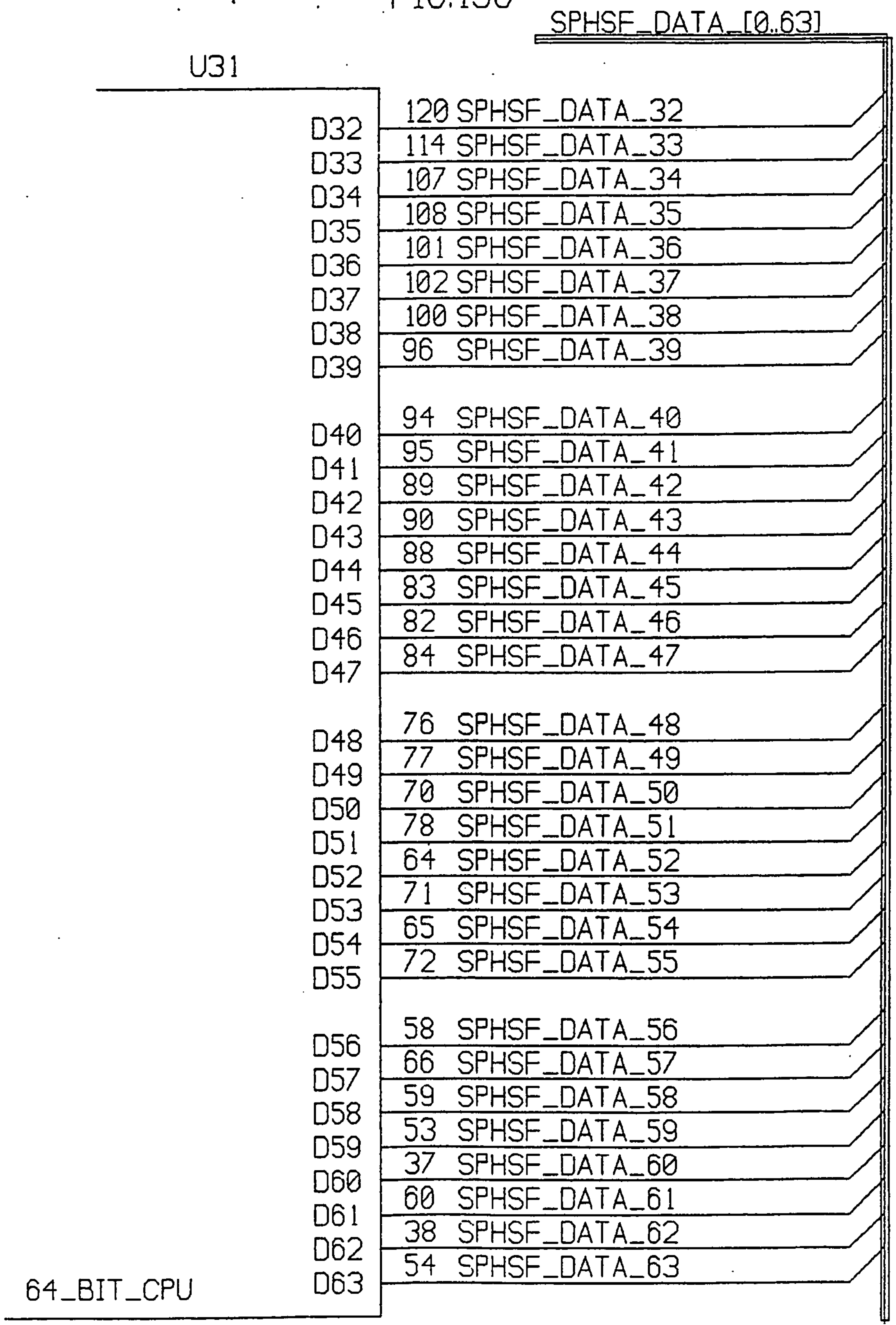
SPECIAL PURPOSE HIGH SPEED FUNCTION

FIG.13B



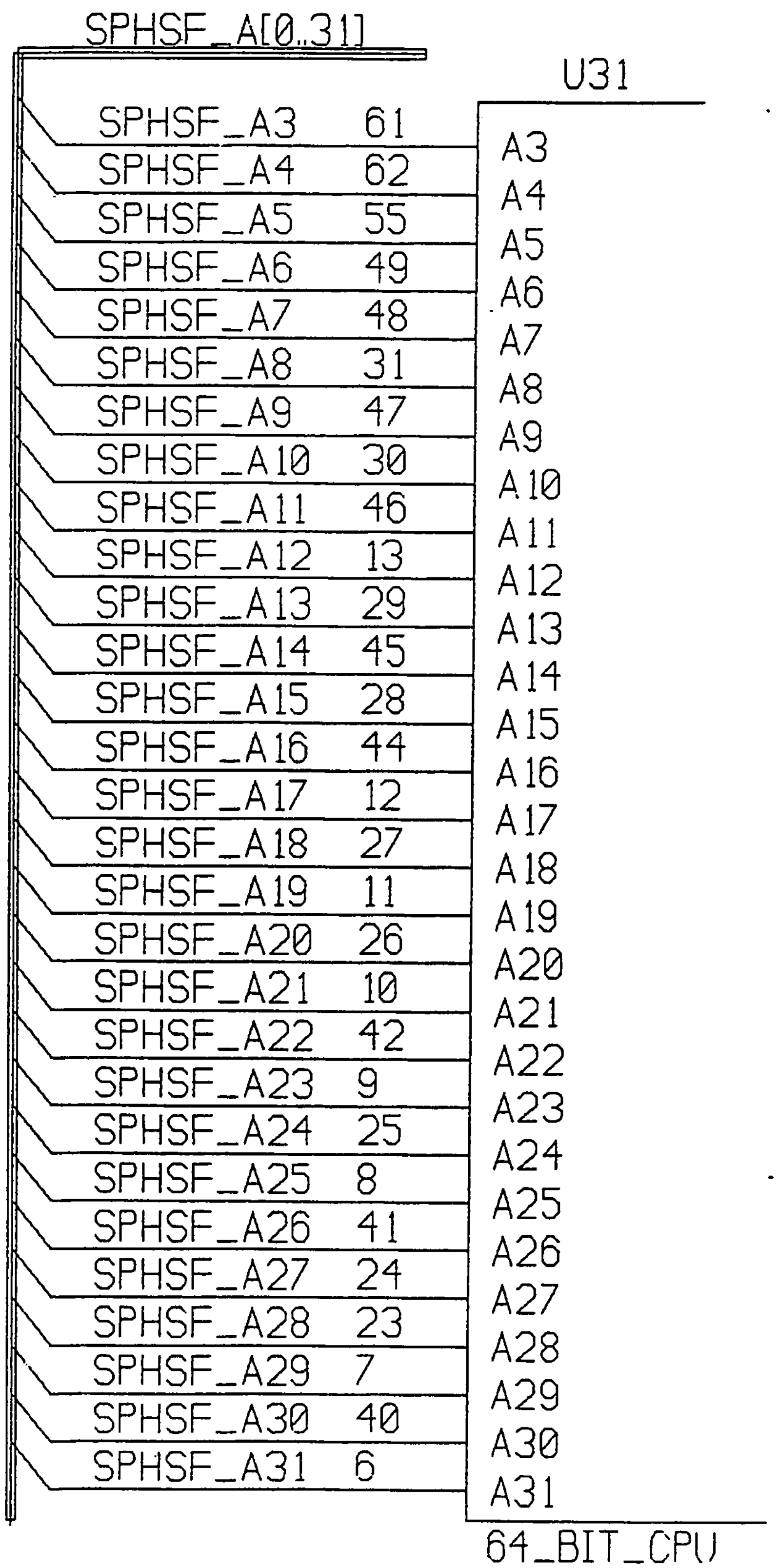
SPECIAL PURPOSE HIGH SPEED FUNCTION

FIG.13C



SPECIAL PURPOSE HIGH SPEED FUNCTION

FIG. 13D



SPECIAL PURPOSE HIGH SPEED FUNCTION

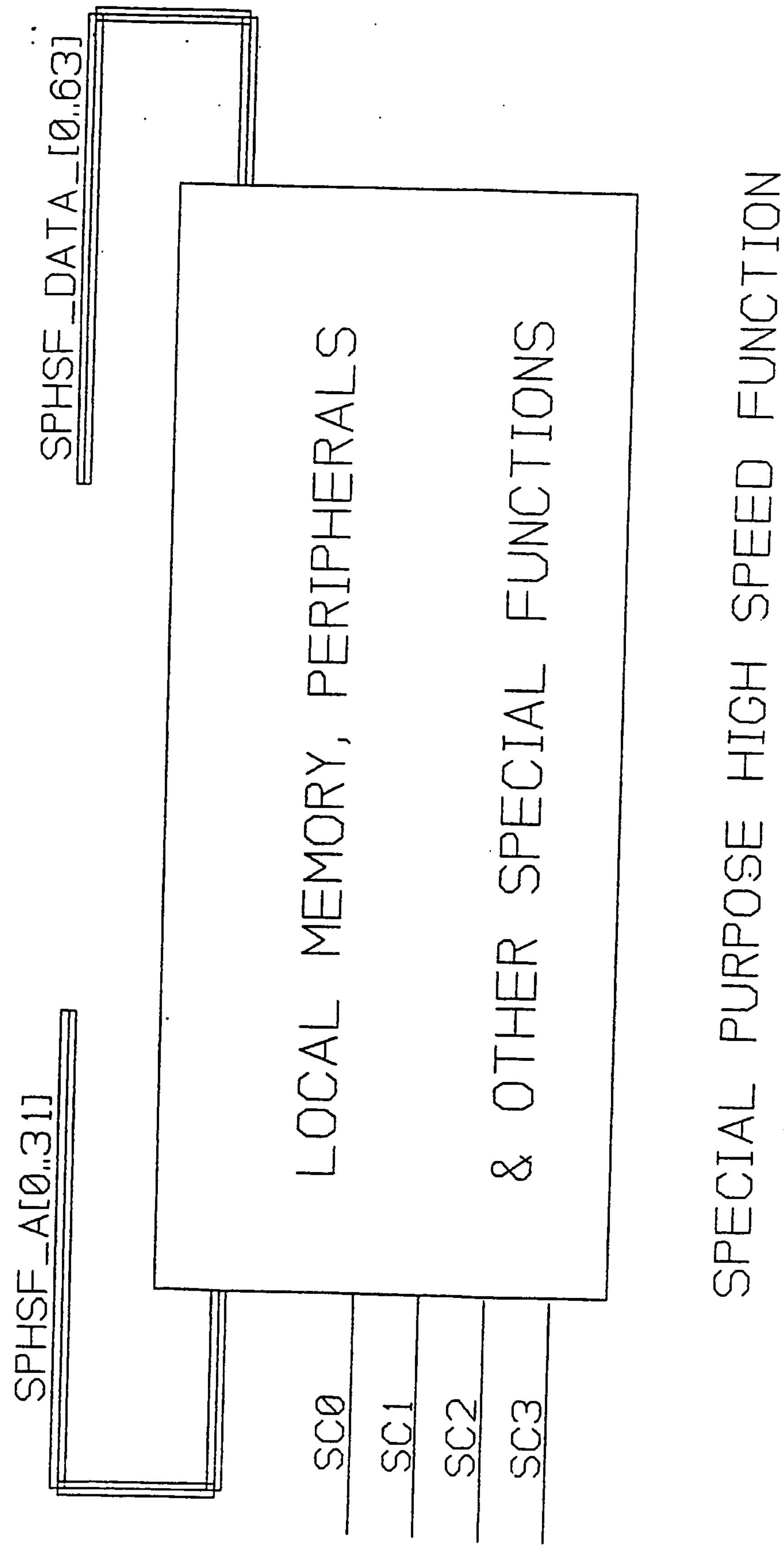

SPHSF_DATA_[0..63]
LOCAL MEMORY, PERIPHERALS
& OTHER SPECIAL FUNCTIONS
SPECIAL PURPOSE HIGH SPEED FUNCTION
SPHSF_A[0..31]
SC0
SC1
SC2
SC3

FIG.13E

INTERNATIONAL SEARCH REPORT

International Application No PCT/US91/05006

I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all) [3]

According to International Patent Classification (IPC) or to both National Classification and IPC

IPC (5): G06F 13/00, 15/20 U.S. Cl. 395/325

II. FIELDS SEARCHED

Minimum Documentation Searched [4]

Classification System	Classification Symbols
U.S. Cl.	395/325,800

Documentation Searched other than Minimum Documentation to the Extent that such Documents are Included in the Fields Searched [5]

III. DOCUMENTS CONSIDERED TO BE RELEVANT [14]

Category *	Citation of Document, [16] with indication, where appropriate, of the relevant passages [17]	Relevant to Claim No. [18]
Y	US, A, 4,246,637 (BROWN) 20 JANUARY 1981 (20.01.81) Note (Fig. 1, element 22; Col. 2, lines 17-20; Col. 3, lines 36-38)	1-11
Y	US, A, 4,860,244 (BRUCKERT) 22 AUGUST 1989 (22.08.89) Note (Abstract; Col. 2 and 3; Fig. 6)	2-6
Y,P	US, A, 4,953,930 (RAMSEY) 04 SEPTEMBER 1990 (04.09.90) Note (Col. 3, lines 18-36; Col. 2, lines 60 and 61; Abstract)	7-9,11
A	US, A, 4,591,973 (FERRIS, III) 27 MAY 1986 (27.05.86)	1-11
A	US, A, 4,309,754 (DINWIDDIE, JR.) 05 JANUARY 1982 (05.01.82)	1-11

* Special categories of cited documents: [15]

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

IV. CERTIFICATION

Date of the Actual Completion of the International Search [2]	Date of Mailing of this International Search Report [2]
22 OCTOBER 1991 (22.10.91)	11 DEC 1991
International Searching Authority [1]	**Signature of Authorized Officer** [20]
ISA/US	Ngoc-Ho Nguyen NGUYEN NGOC-HO INTERNATIONAL DIVISION for GOPAL C. RAY

Form PCT/ISA/210 (second sheet) (May 1986)